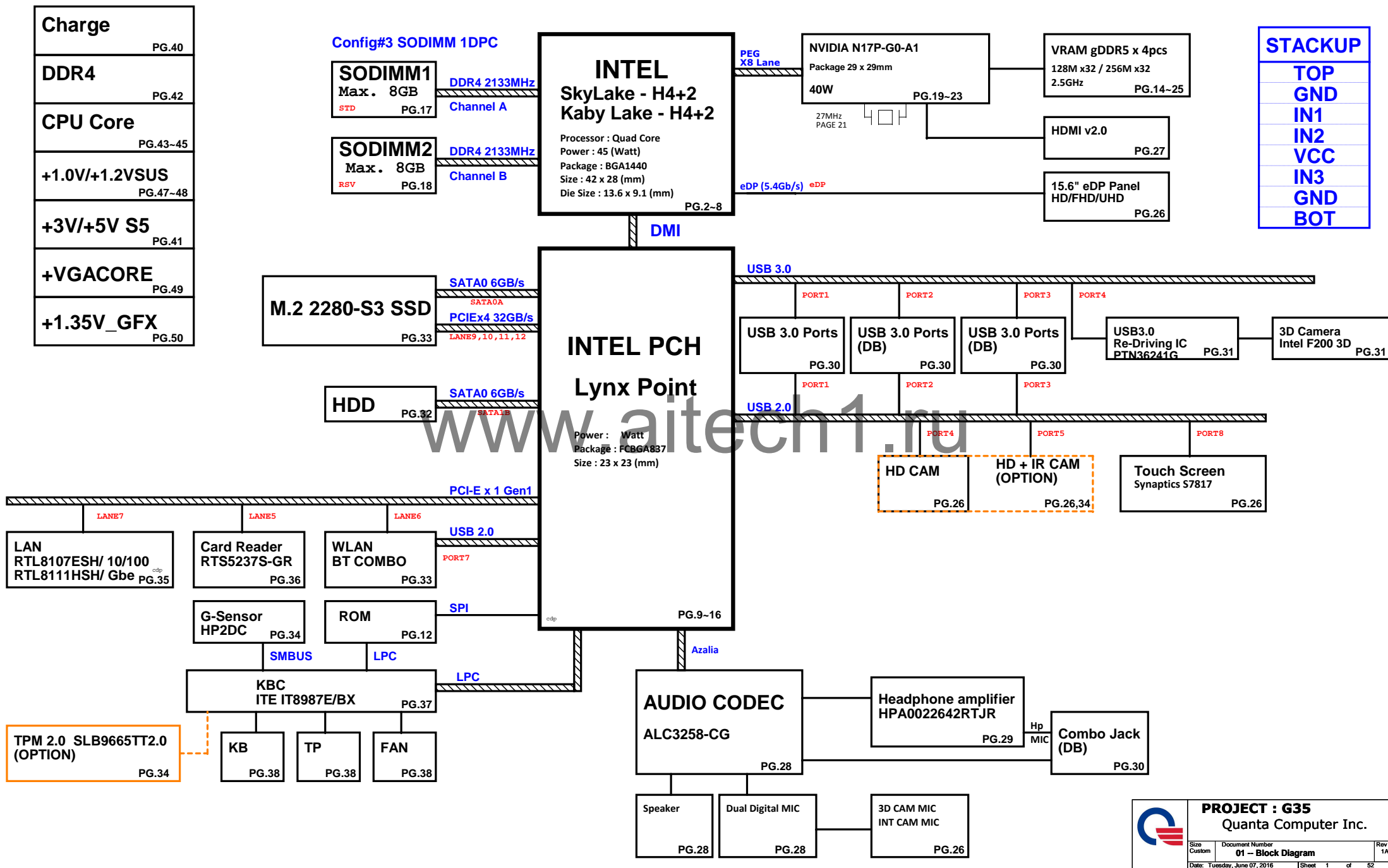
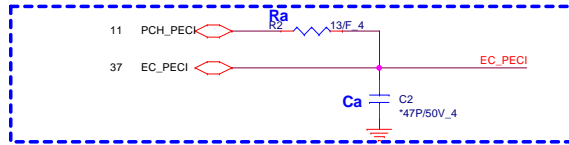


POWER PAVILION Trifle INTEL SKL / KABY -H SYSTEM DIAGRAM

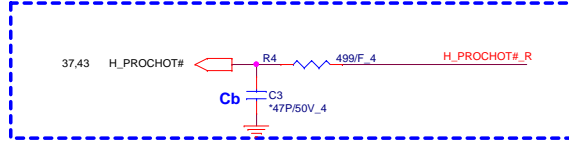
01



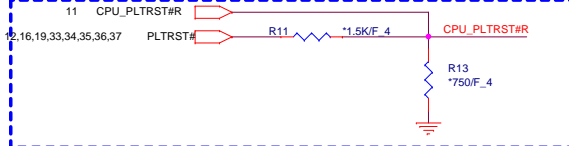
H_PECI (50ohm)
Trace Length: <0.5 inches
Ra,Ca need placement close to PCH.



PROCHOT# (50ohm)
Trace Length <11 inches
Cb need placement near VR

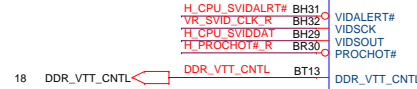
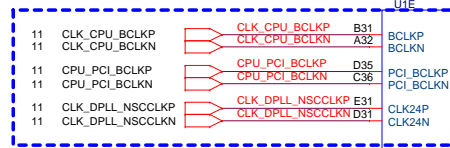


CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches

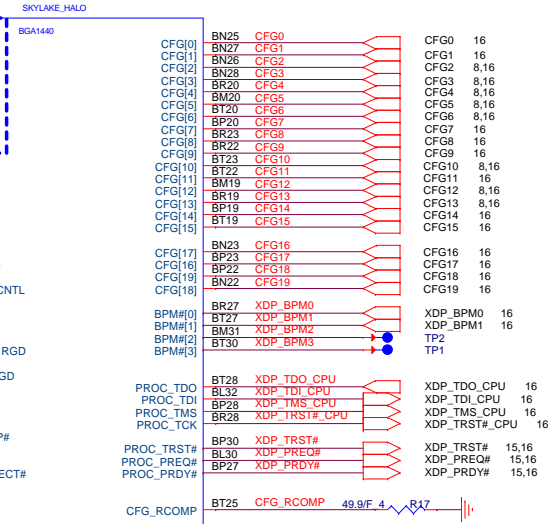
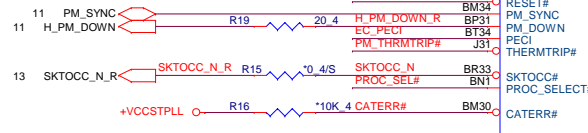


SKYLAKE Processor (CLK,MISC,JTAG)

Host CLK:
Trace length < 11000 mils
Trace spacing = 15 / 20 mils, Impedence 90 ohm

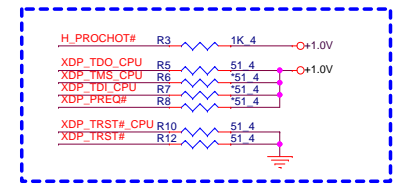


PM_SYNC (50ohm)
Trace Length: 1~11.25 inches



Design Note(CFG_RCOMP):
DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)

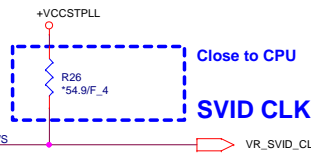
Processor pull-up (CPU)



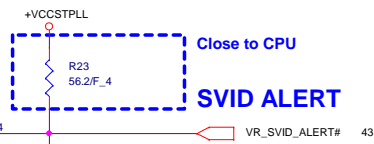
CPU CORE SVID

Layout note:
1.Need routing together
2.ALERT need between CLK and DATA.

PLACE THE PU RESISTORS
CLOSE TO VR
PULL UP IS IN THE VR MODULE



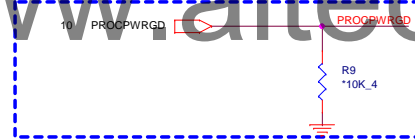
CLOSE TO CPU
PLACE THE PU RESISTORS



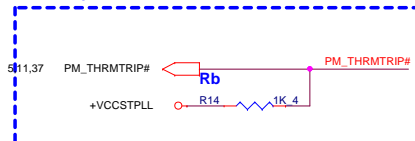
CLOSE TO CPU
PLACE THE PU RESISTORS



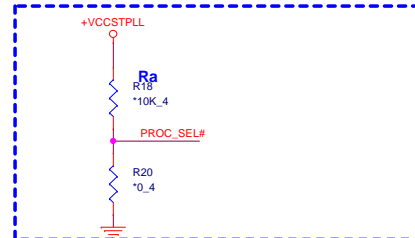
PROC_PWRGD (50ohm)
Trace Length: 1~11.25 inches



THERMTRIP# (50ohm)
Trace Length: 1.1~12 inches
Rb need placement near PCH

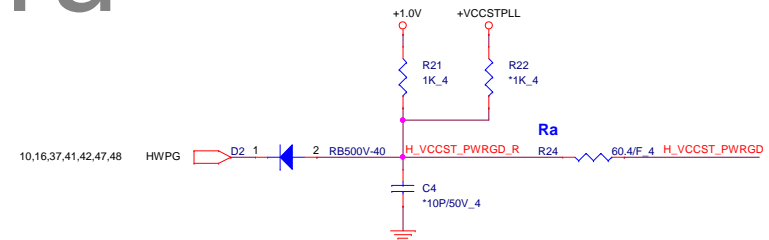


Ra(R10804) Not install in SKL-H



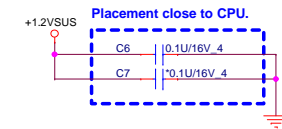
HWPD

Ra close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"



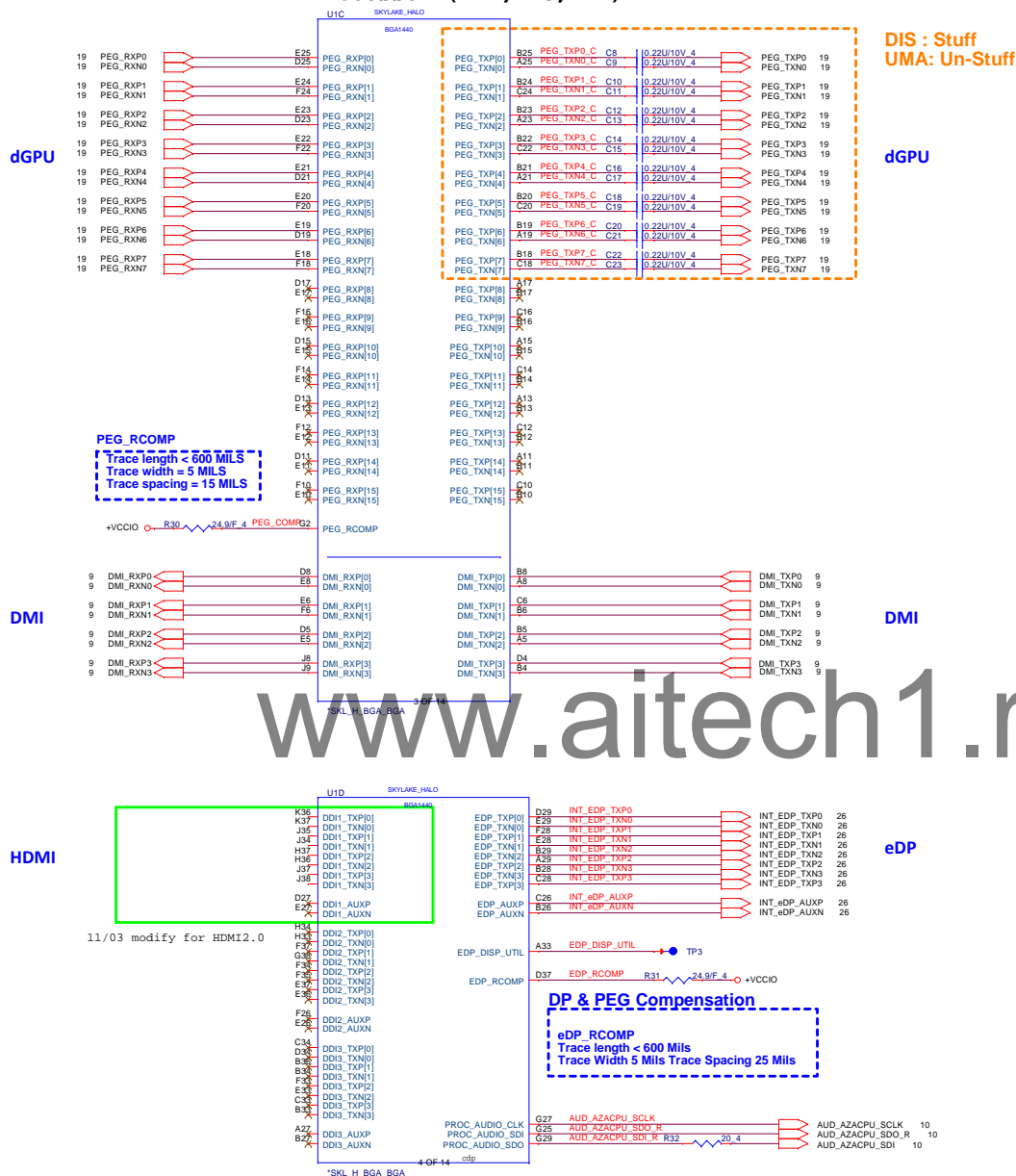
CPU VDDQ

Note: please keep plane is enough for VDDQ 2.8A

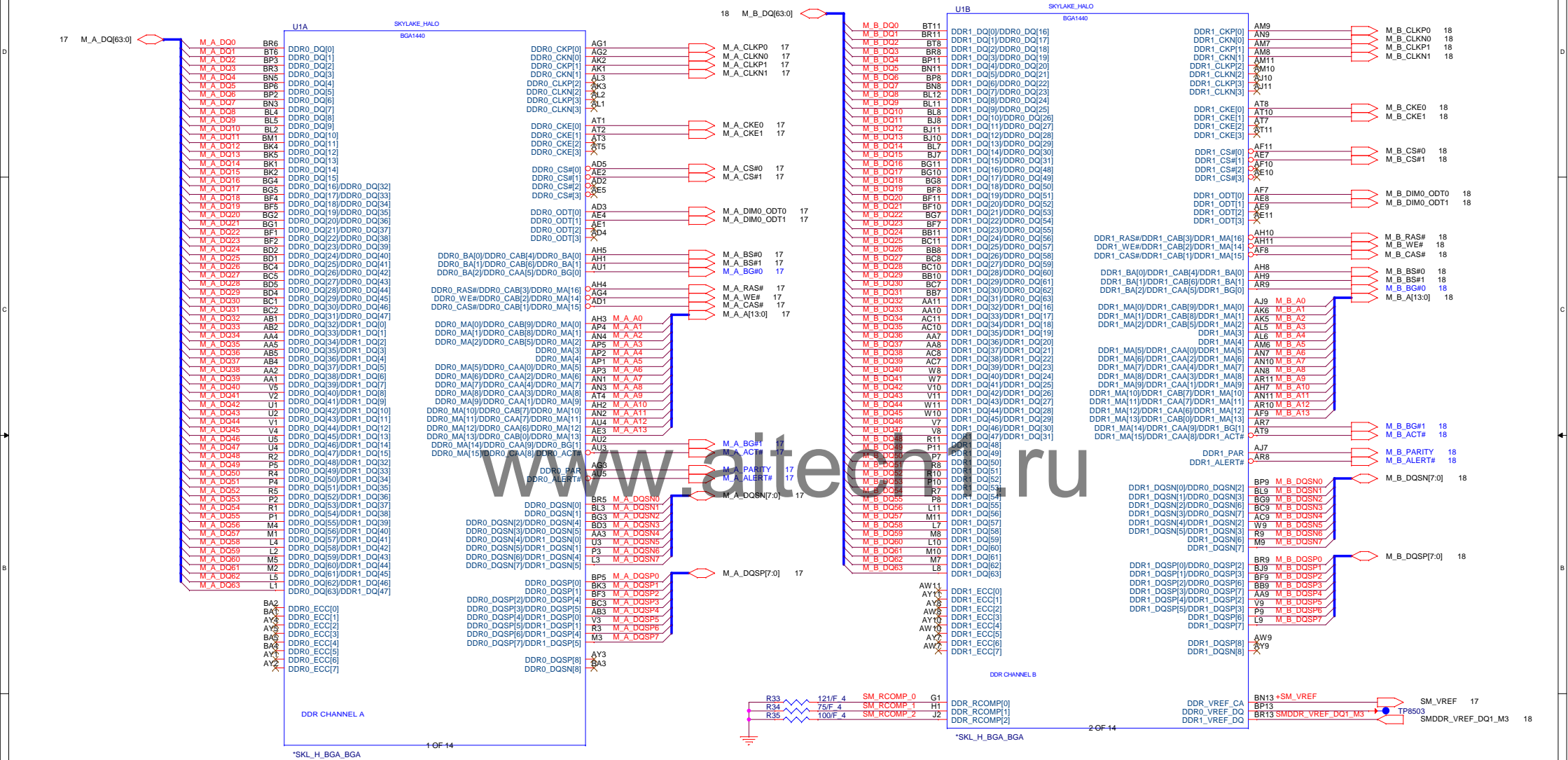


SKYLAKE Processor (DMI,PEG,FDI)

03



SKYLAKE Processor (DDR4)



Follow SKL H EDS page 133 to 45W(GT2): +VCCGT=55A

+VCC CORE 7.43,44
+1.2VSUS 2.6,10,17,18,42,48,51



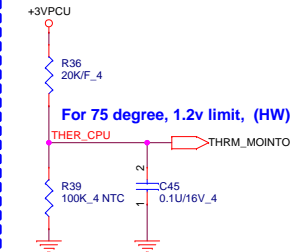
14 OF 14

*SKL_H_BGA_BGA

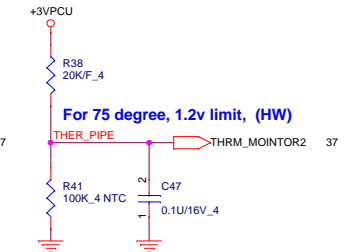
IO Thrm Protect

Location need thermal confirm

For CPU USE

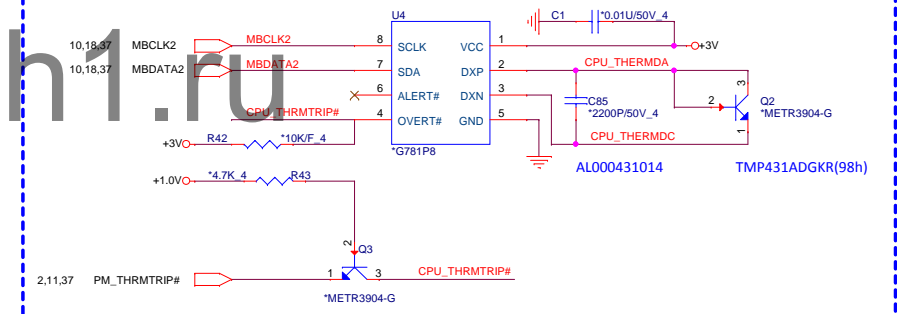


For PIPE USE

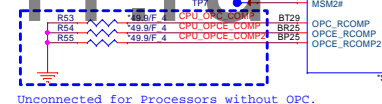


CPU Thermal Sensor

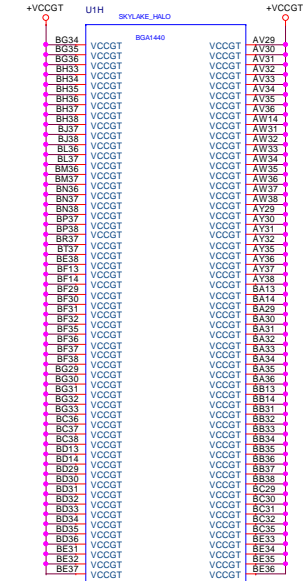
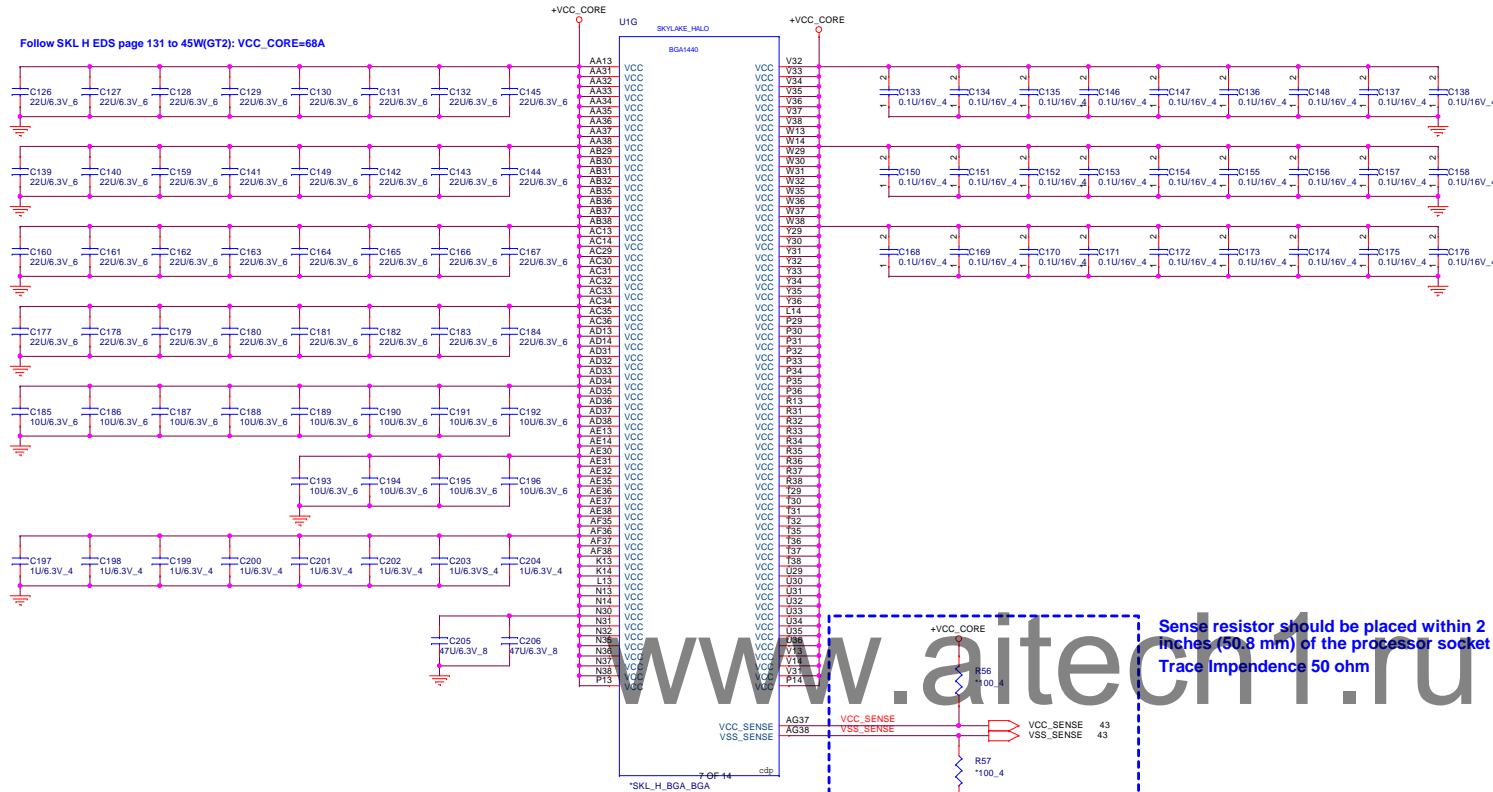
Location need thermal confirm



Follow SKL H EDS page 135 45W: VDDQ=2.8A



Follow SKL H EDS page 131 to 45W(GT2): VCC_CORE=68A



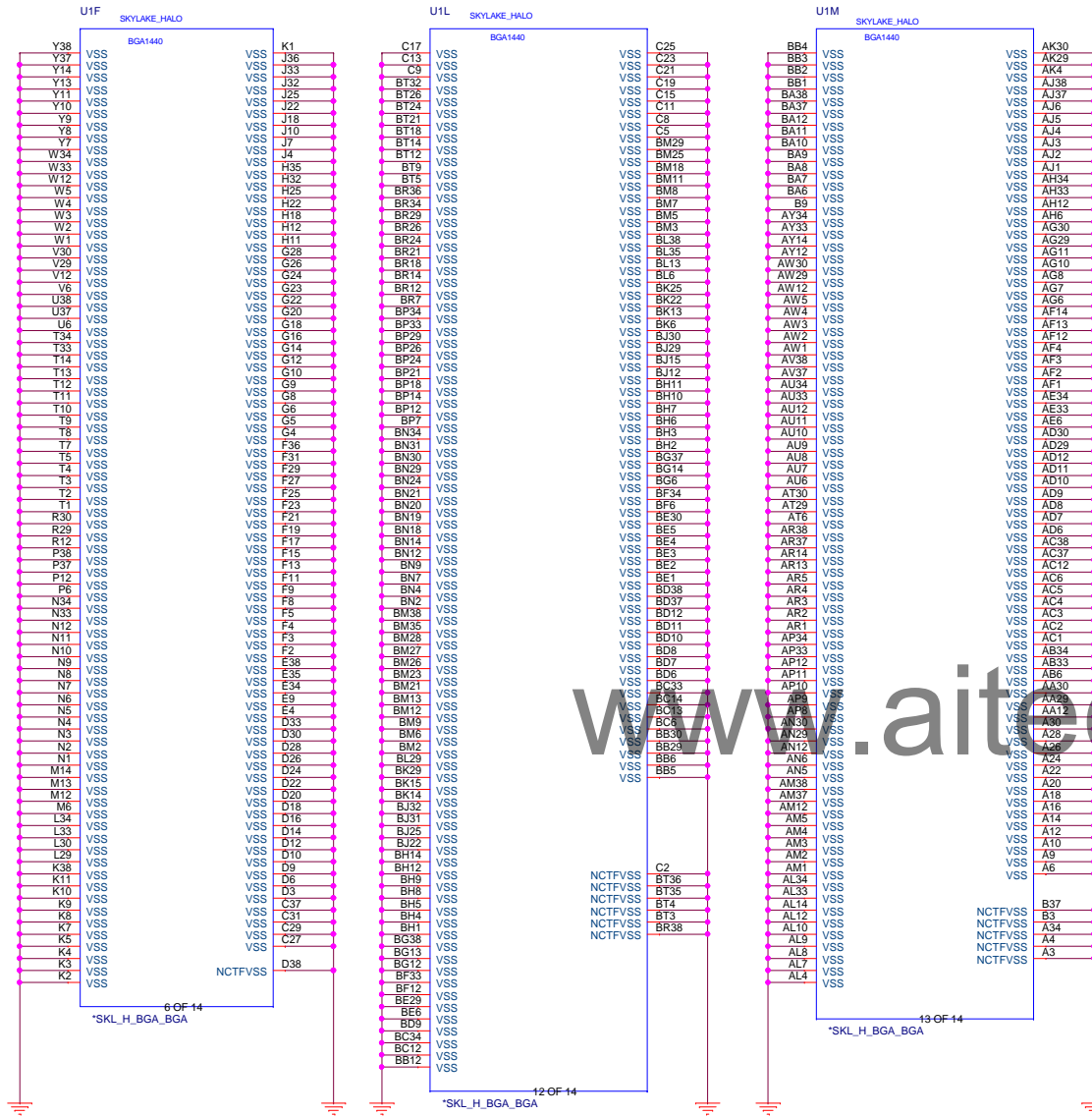
+VCC_CORE 43.44



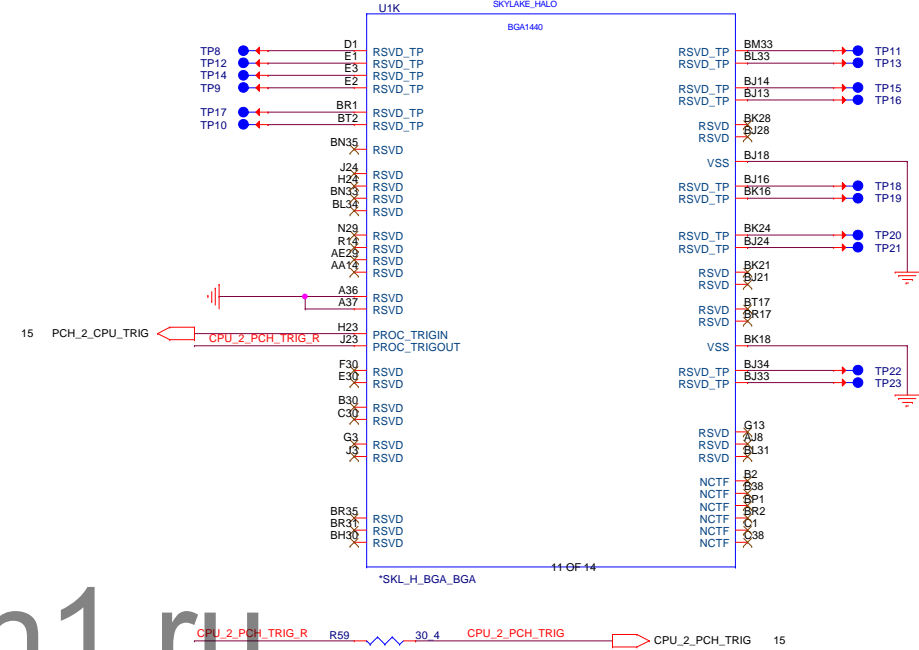
PROJECT : G35
Quanta Computer Inc.

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SKL-HProcessor (GND)



SKL-H Processor (RESERVED, CFG)

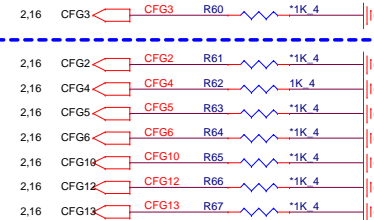


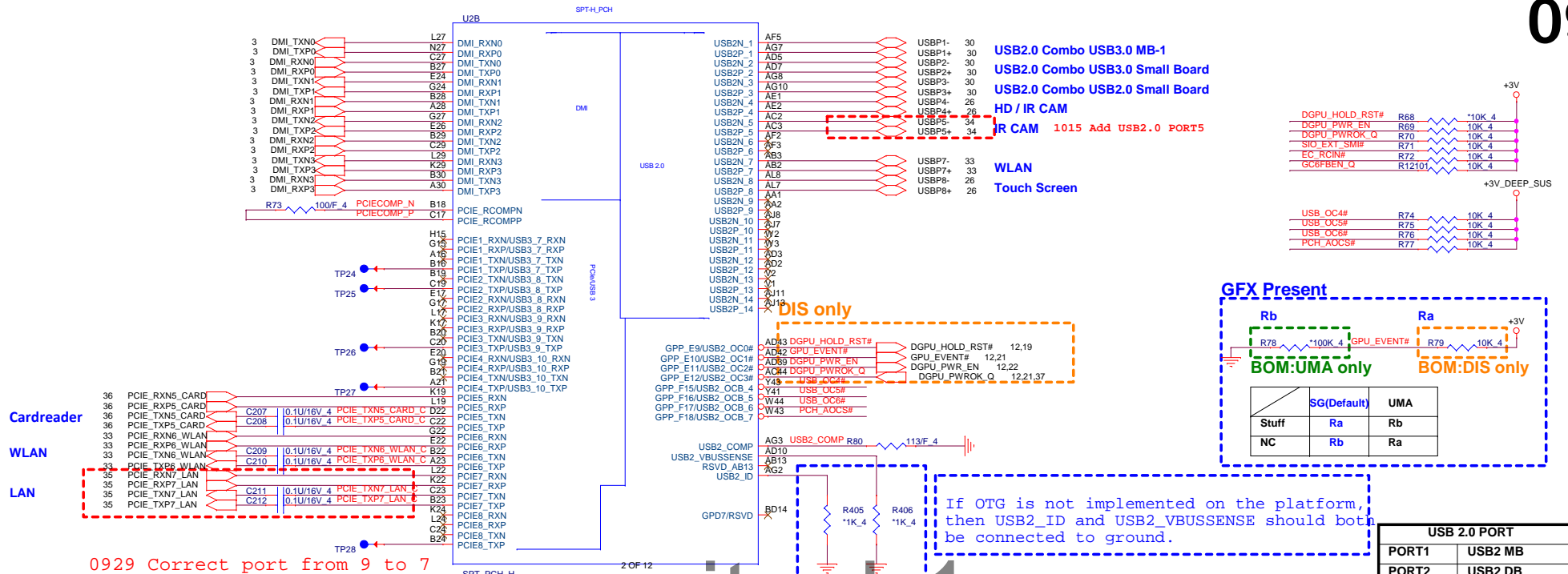
Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

0 Enable; SET DFX_ENABLED BIT IN DEBUG

1, Disable;





USB 2.0 PORT	
PORT1	USB2 MB
PORT2	USB2 DB
PORT3	USB2 DB
PORT4	HD/IR CAM Option
PORT5	IR CAM Option
PORT6	NC
PORT7	WLAN
PORT8	TOUCH
PORT9-14	NC

USB 3.0 PORT	
PORT1	USB3 MB
PORT2	USB3 DB
PORT3	USB3 DB
PORT4	3D CAMERA

10,12,13,14,16,18 +3V_DEEP_SUS

HSIO MUX PORT	
PCIE1-4	NC
PCIE5	Cardreader
PCIE6	Wlan
PCIE7	Lan
PCIE8	NC
PCIE9/SATA0A	SSD PCIE * 4
PCIE10	
PCIE11	
PCIE12	
PCIE13	NC
PCIE14	NC
PCIE15	HDD
PCIE16	NC
PCIE17	NC
PCIE18-20	NC

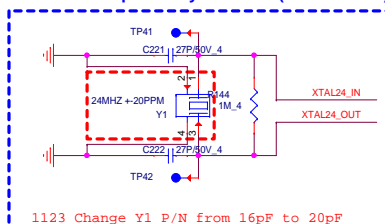
SSD PCIE x4 LANE

Modify 1005 Change HDD SATA Port2 to port1B

HDD1 (SATA1B 6Gb/s)

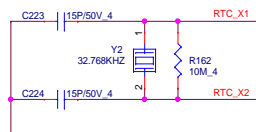
SSD PCIE x4 LANE

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-H needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-H.

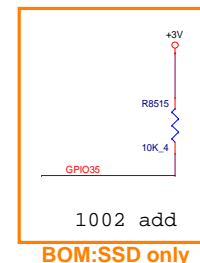
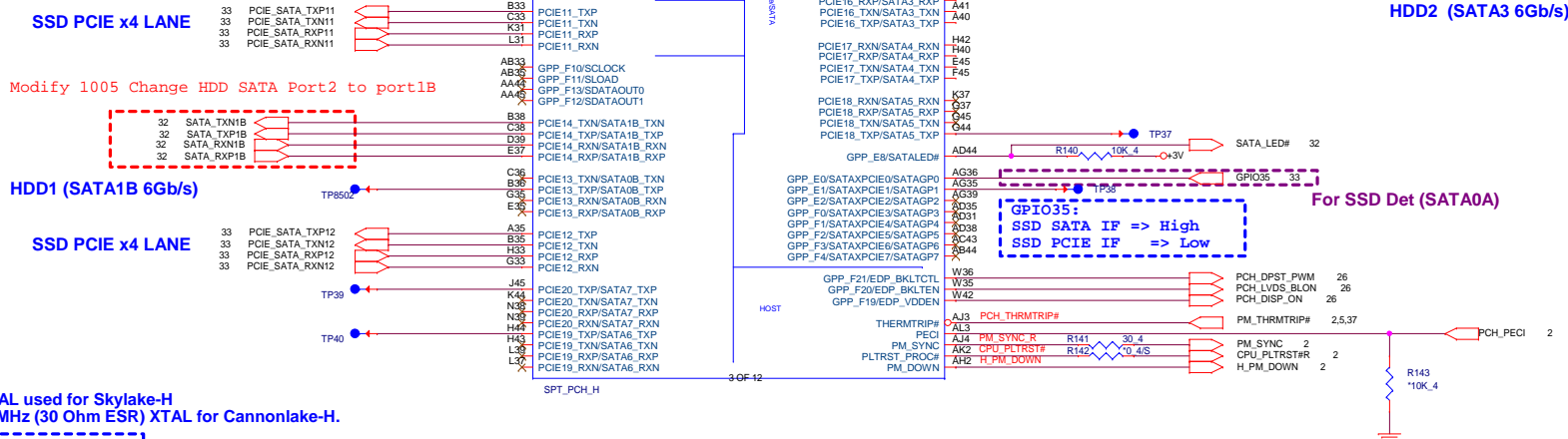


Crystal Components with Surrounding 10 mil Wide GND Shield Trace
Break Out: 4-10 mil Wide GND Shield Trace

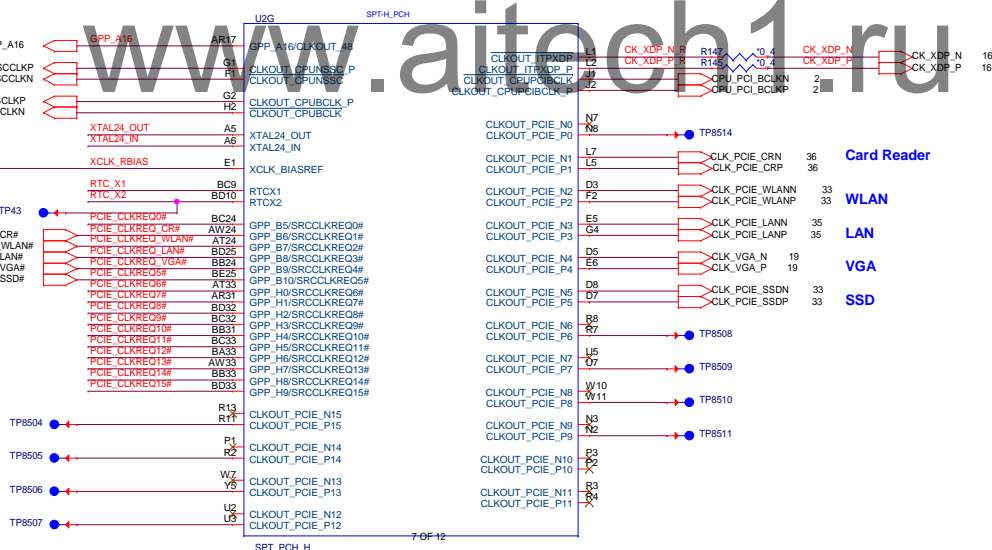
RTC Clock 32.768KHz

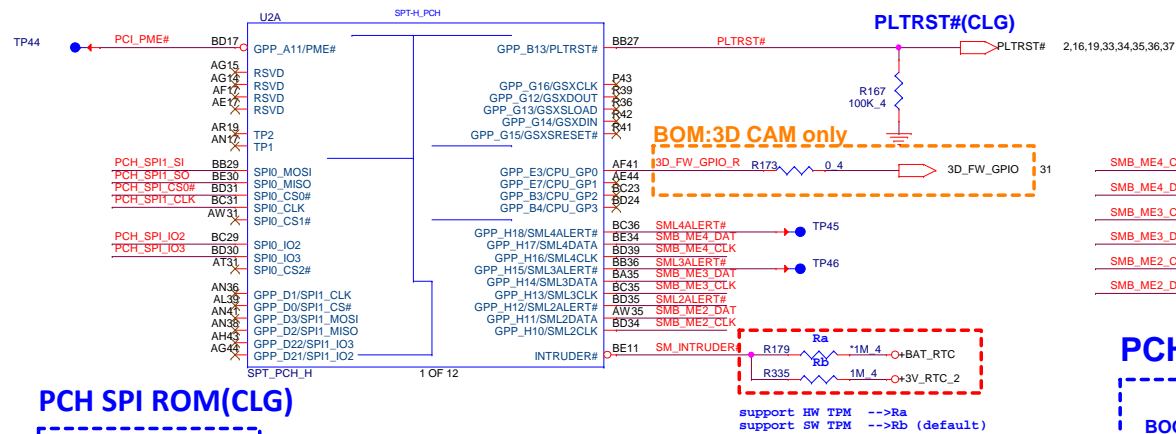


32.768KHz
BG332768453 CRYSTAL SMD 32.768KHZ(+/-20PPM,12.5PF)
footprint: xtl-3_2X1_5-2_5-0_8h



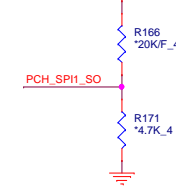
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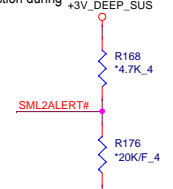
RESERVED

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



ESPI FLASH SHARING MODE

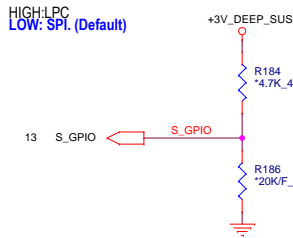
HIGH: SLAVE ATTACHED FLASH SHARING
LOW: 0: MASTER ATTACHED FLASH SHARING
This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.



PCH Strap Pin

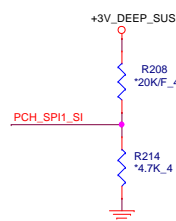
BOOT SELECT STRAP

HIGH: LPC
LOW: SPI (Default)

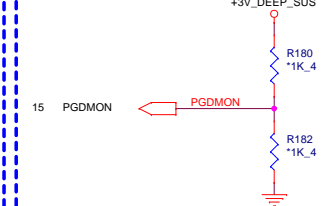


RESERVED

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

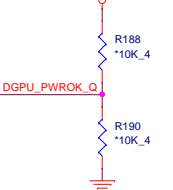


DFX TEST MODE QUALIFIER FOR OTHER DFX STRAP WHEN SAMPLED LOW



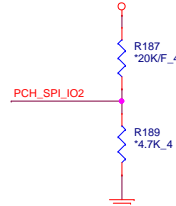
DFX TEST MODE

XTAL INPUT IS SINGLE ENDED IF SAMPLED LOW ELSE DIFFERENTIAL



RESERVED

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

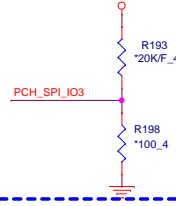


RING OSCILLATOR BYPASS



RESERVED

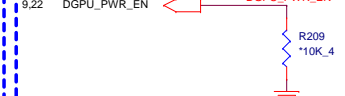
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



XTAL INPUT FREQUENCY[0]

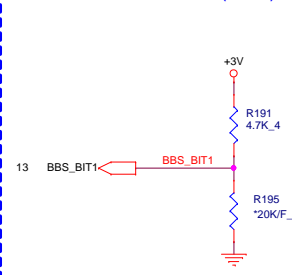


XTAL INPUT FREQUENCY[1]



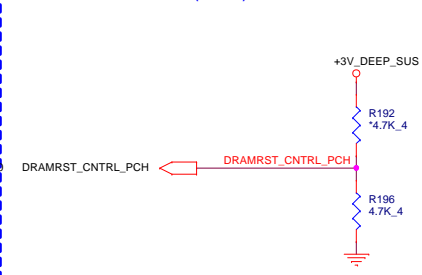
NO REBOOT IF SAMPLED HIGH

HIGH: TOP SWAP ENABLED (CRB)
LOW: Disable "No Reboot" mode. (Default)



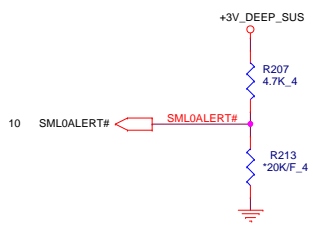
ESPI/LPC SELECT STRAP

HIGH: ESPI is selected for EC.
LOW: LPC is selected for EC. (Default)



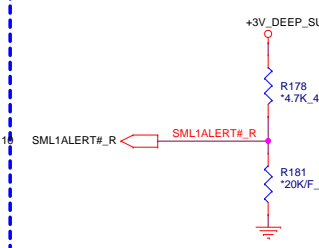
TLS CONFIDENTIALITY ENABLED

HIGH: T Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). (CRB)
LOW: Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)



RESERVED

This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.

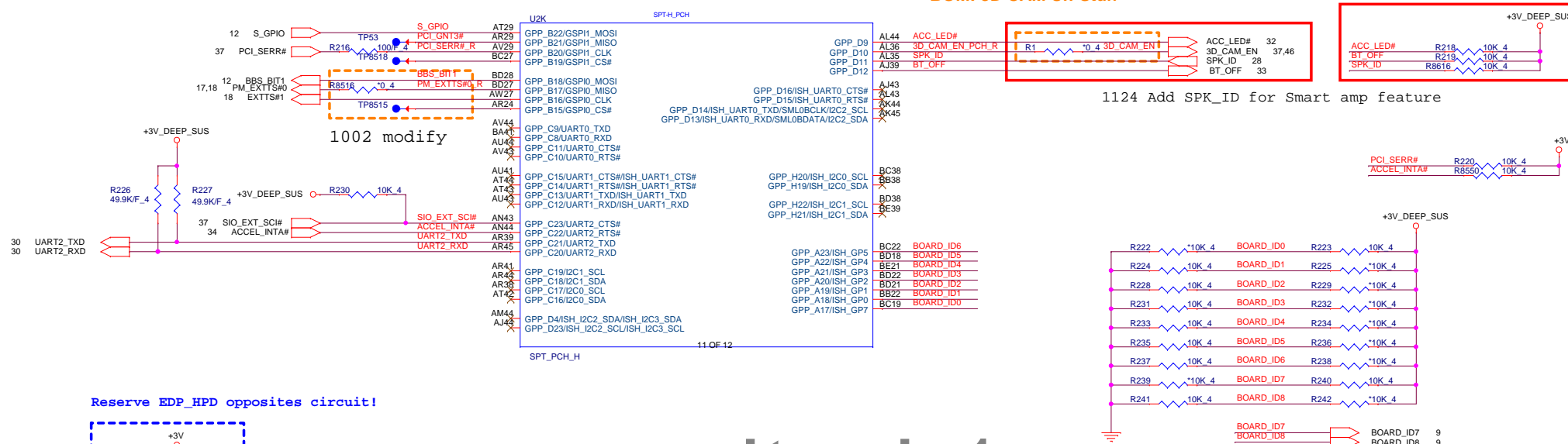


Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

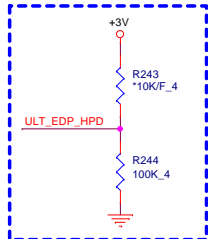


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Size	Document Number	Rev
Custom	12 - PCH 4/7 (GPIO/MISC)	1A
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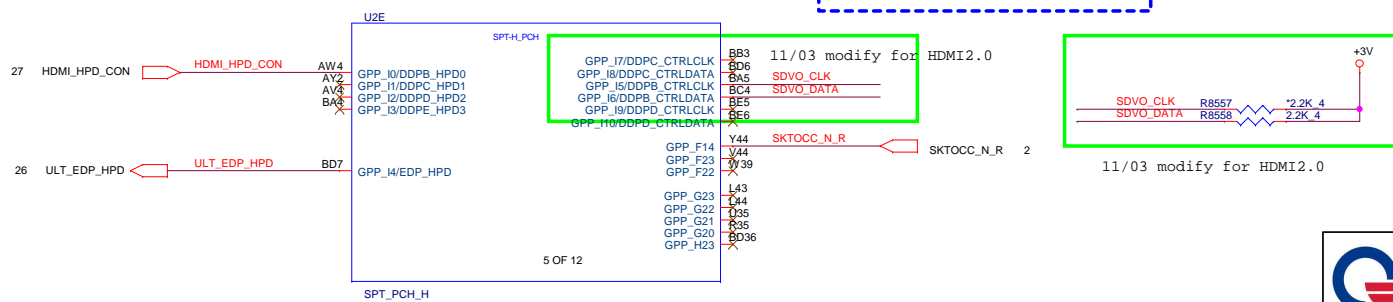
Reserve EDP HPD opposites circuit!

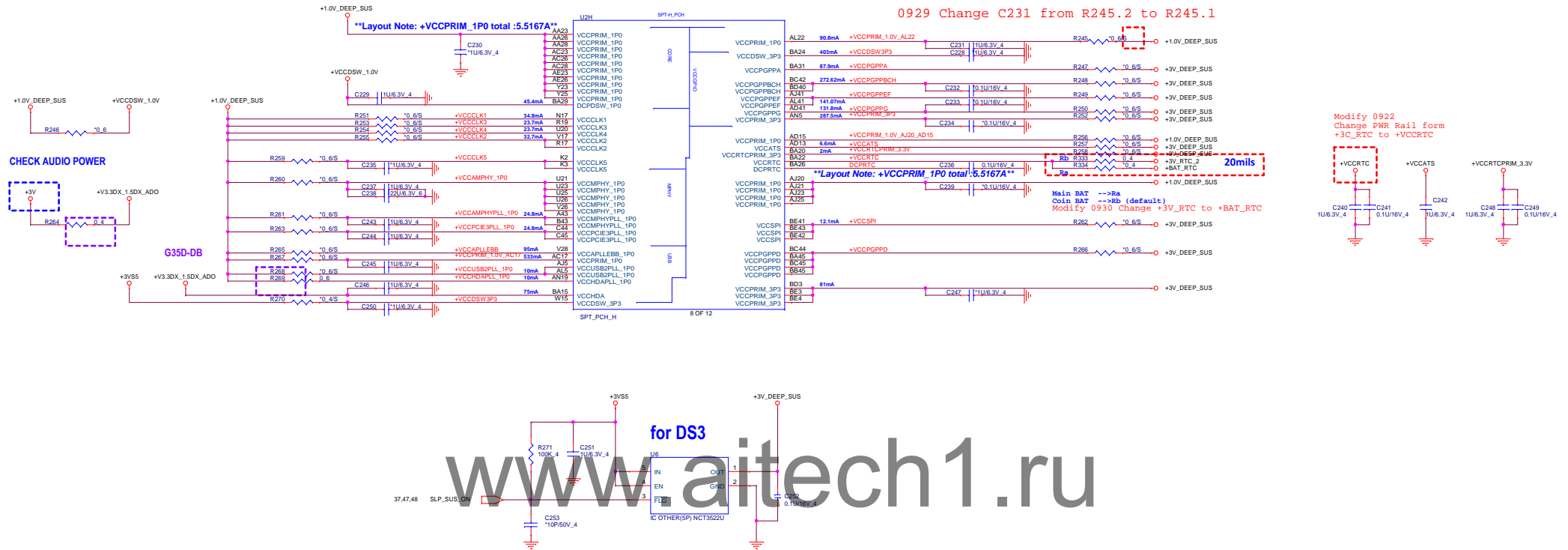


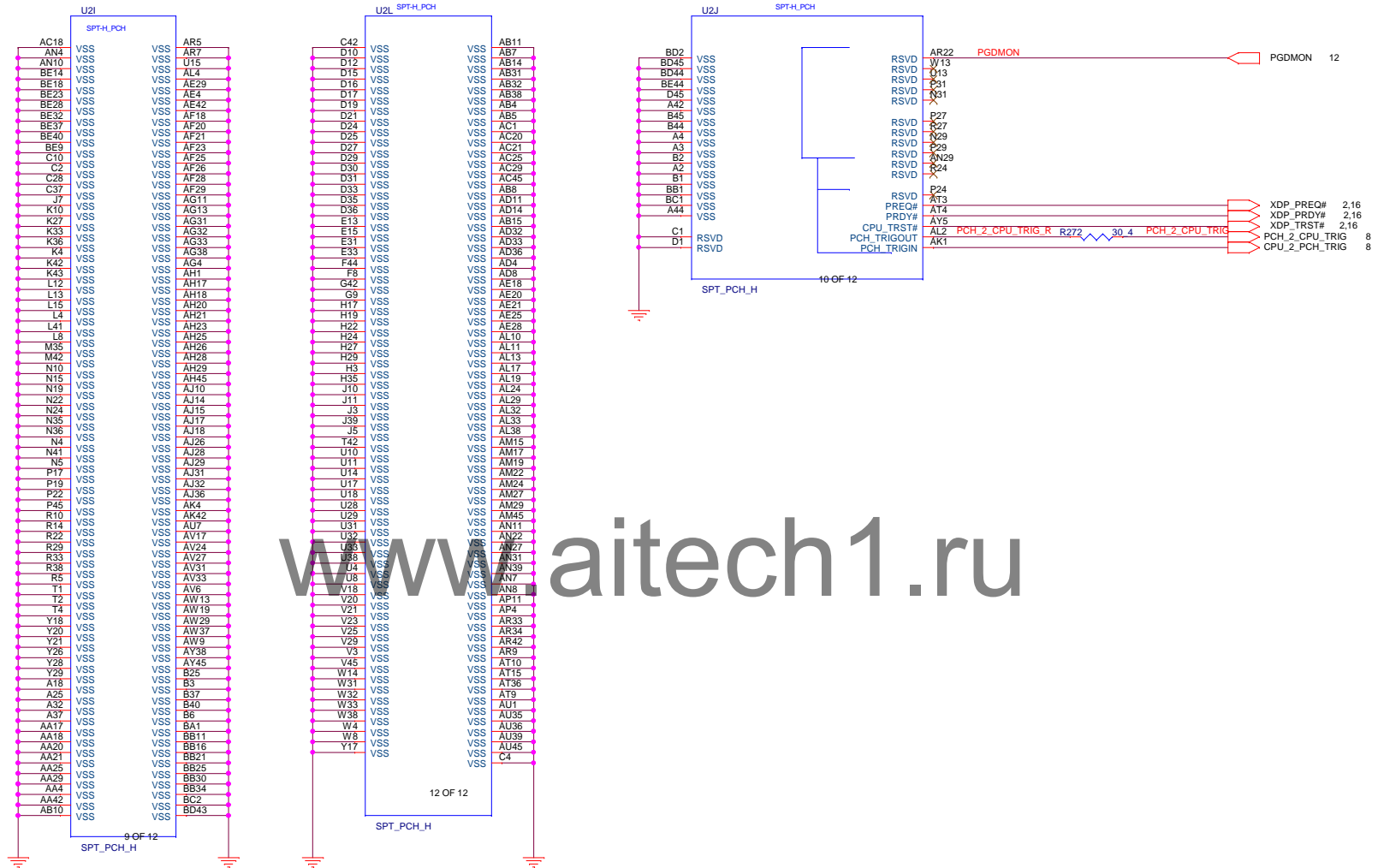
Model: BOARD_ID[8:7]

Model	BOARD_ID[8:7] ID8;ID7	BOARD_ID[6:5] ID6;ID5	Board ID [4:3] ID4;ID3		BOARD_ID[2:1] ID2;ID1	BOARD_ID0 ID0
Definition	01 SKL H 10 KBL H *RSV	00 Reserve	ID4 Reserve	ID3 0 Nvidia 1 AMD	00 15" 01 17" 10 17" SP	0 : UMA 1 : DIS

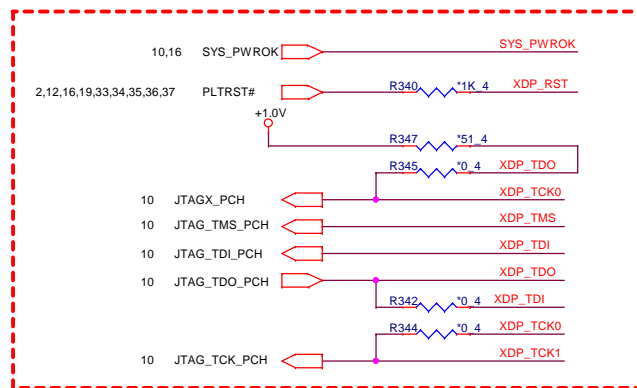
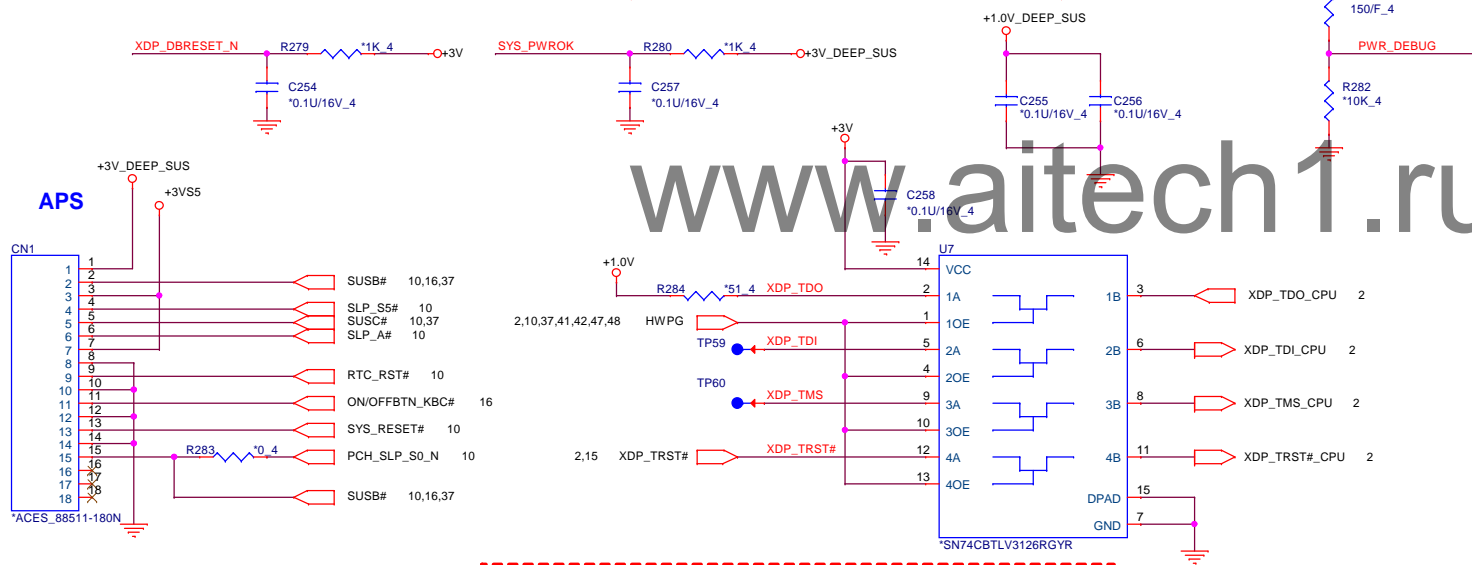
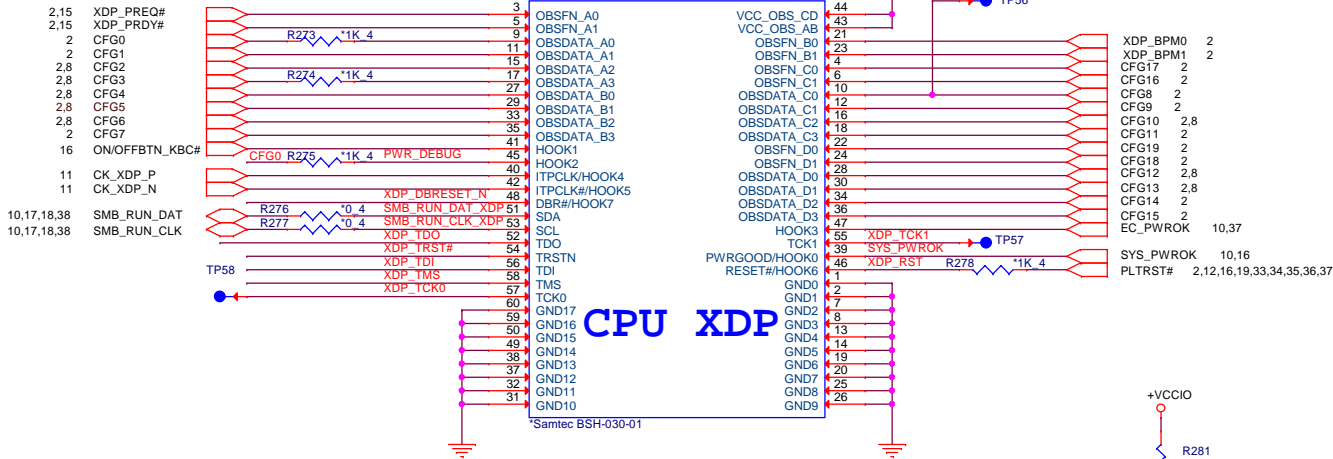
This signal has a weak internal pull-down.
0 = Port C and D is not detected.
1 = Port C and D is detected.



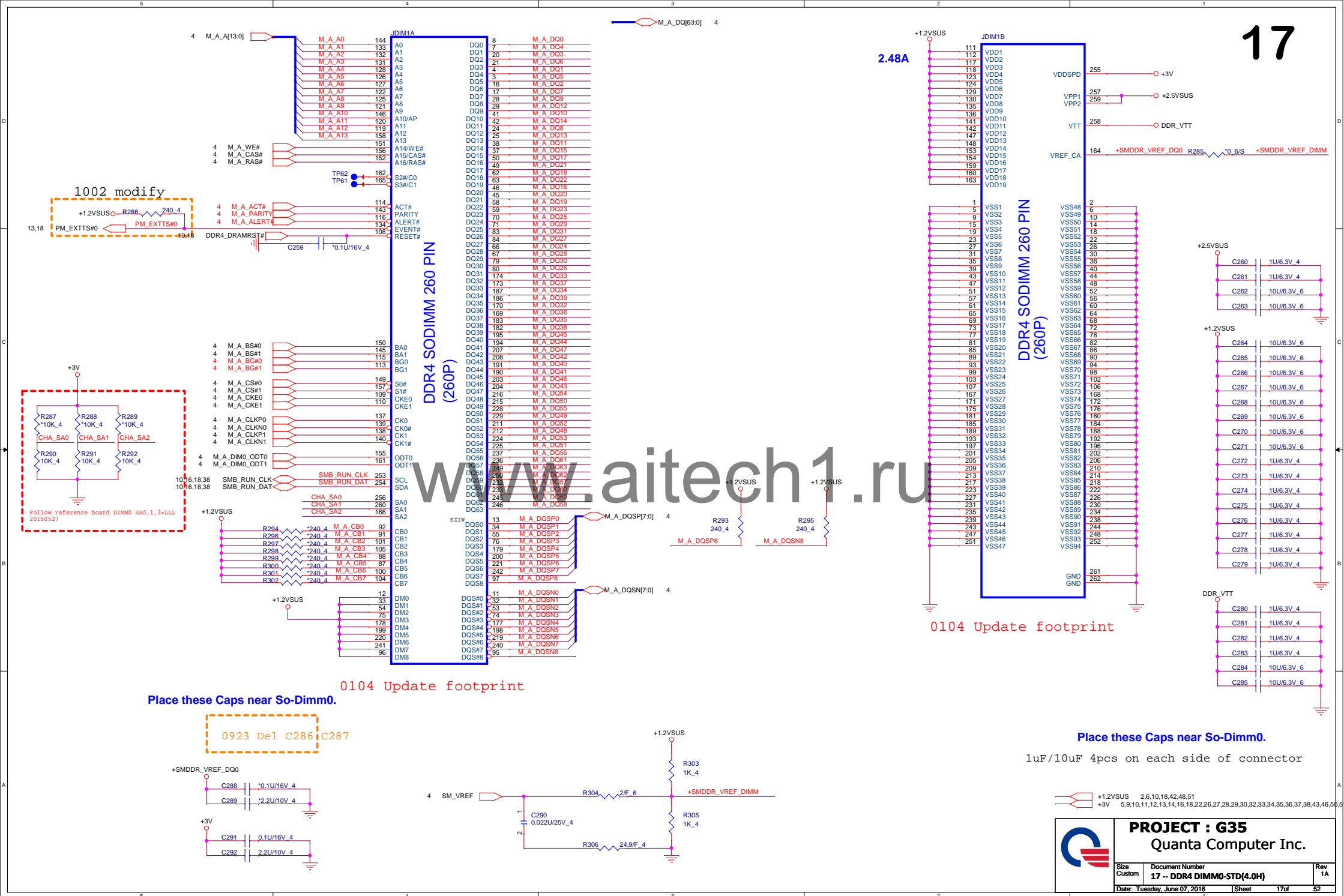


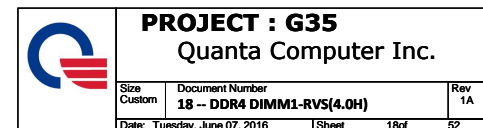


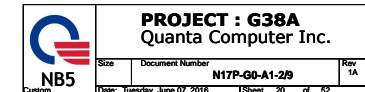
+3VS5 10,12,14,33,37,41,42,46,47,48
 +3V_DEEP_SUS 9,10,12,13,14,18
 +3V 5,9,10,11,12,13,14,17,18,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,50,51
 +1.0V_DEEP_SUS 10,11,14,47,48
 +VCCIO 3,6,48
 +1.0V 2,5,6,10,37,48

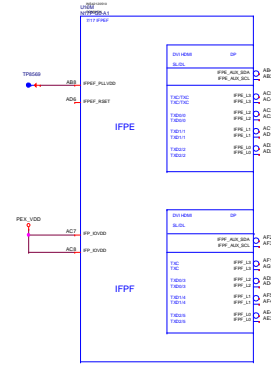
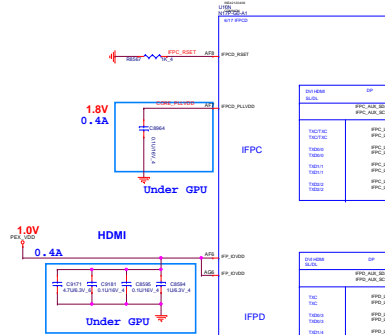
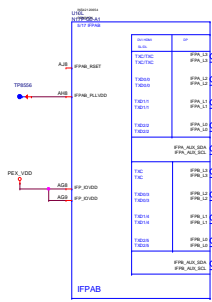


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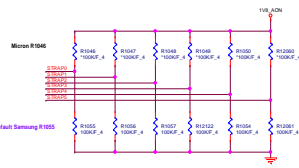




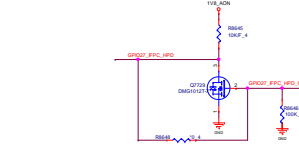
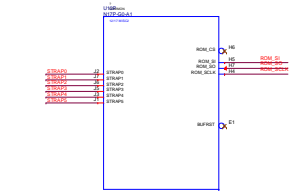
STRAP[2:0] VRAM Table for N17P-G0 GDDR5 Recommended Memories

STRAP[2:0]	Memory	Vendor	Part No.	Temp. R/W	Q/R P/W
000	GDDR5 2048x128 Gbit	Samsung	K4G221257E-BC28	AXG5G0U7B	AXG5G0U7B
001	GDDR5 2048x128 Gbit	Micro A die	MT51L256K32B-701A	AXG5G0U7B	AXG5G0U7B
002	GDDR5 2048x128 Gbit	Hynix M die	H5GC4824N9R-BC	AXG5G0U7B	AXG5G0U7B
003	GDDR5 2048x128 Gbit	Samsung E die	K4G41325P-BC28	AXG5G0U7B	AXG5G0U7B
004	GDDR5 2048x128 Gbit	Micro A die	MT51L256K32B-701A	AXG5G0U7B	AXG5G0U7B
005	GDDR5 2048x128 Gbit	Hynix M die	H5GC4824N9R-BC	AXG5G0U7B	AXG5G0U7B

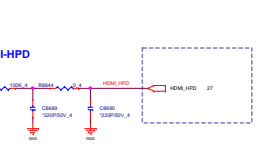
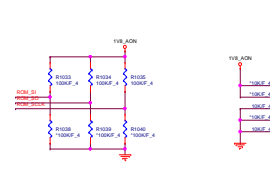
Vendor	Size	PN
Vendor	Size	PN
Vendor	Size	PN



Default Samsung R100



Vendor	Size	PN
Vendor	Size	PN
Vendor	Size	PN



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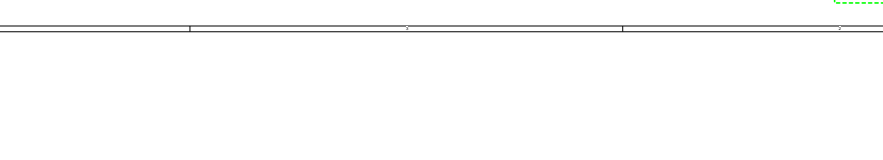
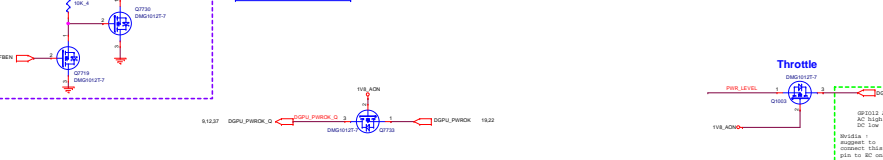
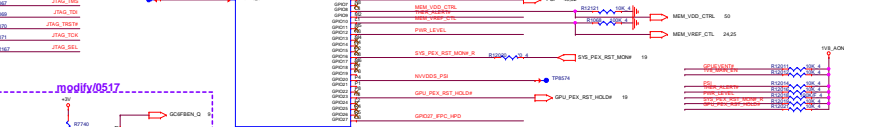


Table 14.2 GPIO Descriptions for GB4C-128 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	HYVDD_PWN_VDD	O	PWM Output to control HYVDD	0 to VDD_PWN output
GPIO1	GCAM_GCA_FB_EN	O	FB Enable for GCA 2.1	Open Source
GPIO2	GCAM_GPU_EVENT_WAKE	I	GPU wake signal for GCA 2.1	10K pull-up to VDD_ACH unless driven actively
GPIO3	HYVDD_SRAM_PWN	O	PWM output to control the SRAM power supply	0 to VDD output
GPIO4	GCAM_VIB_MAH_EN	O	GPU power sequencing for GCA 2.1	Open Drain
GPIO5	FRA_LCK	I	Active low Frame Lock	Open Drain

Table 14.2 GPIO Descriptions for GB4C-128 Packages (Continued)

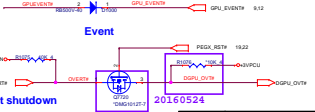
GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO6	HYVDD_FSI	O	Flash Shimming (see Section 14.3.3)	10 K pull-up to VDD_ACH to enable multiple phases
GPIO7	LCD_BL_PWM	O	Panel Backlight enable	10 K pull-up to VDD_ACH
GPIO8	MEM_VDD_CTL	O	Memory voltage control	10 K pull-up to VDD_ACH
GPIO9	THERMAL_ALERT	I/O	Active Low Thermal Alert	Open Drain
GPIO10	MEM_VDD_CTL	O	Memory voltage control	10 K pull-up to VDD_ACH
GPIO11	LCD_VDD	O	Quadro-power enable	100 K pull-up to VDD_ACH
GPIO12	PWR_LEVEL	I	Power supply level	100 K pull-up to VDD_ACH
GPIO13	LCD_BLEN	I	LCD Backlight Enable	Panel Backlight Enable
GPIO14	HPO_IPFA	I	Hot Plug Detect for IPFA	Inverted Input. See Figure 14.5
GPIO15	HPO_IPFE	I	Hot Plug Detect for IPFE	Inverted Input. See Figure 14.5
GPIO16	GCAM_GPU_RST_NOM	I	System side GPU reset monitor	10 K pull-up to VDD_ACH unless actively driven
GPIO17	HPO_IPFD	I	Hot Plug Detect for IPFD	Inverted Input. See Figure 14.5
GPIO18	HPO_IPFE	I	Hot Plug Detect for IPFE	Inverted Input. See Figure 14.5
GPIO19	3D_VISION_L/R	O	3D Vision L/R Signal	100 K pull-up to VDD_ACH
GPIO20	CLK_MODE	I/O	CLK Mode	
GPIO21	UNUSED	I/O	UNUSED	
GPIO22	UNUSED	I/O	UNUSED	

Table 14.2 GPIO Descriptions for GB4C-128 Packages (Continued)

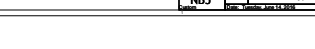
GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO23	GPU_PEX_RST_HOLD	O	GPU PCIe self-reset control	Open Drain
GPIO24	HPO_IPFF	I	Hot plug detect for IPFF	10 K pull-up to a gated VDD
GPIO25	UNUSED	I/O	UNUSED	
GPIO26	UNUSED	I/O	UNUSED	
GPIO27	HPO_IPFC	I	Hot plug detect for IPFC	Inverted Input. See Figure 14.5

Table 14.2 GPIO Descriptions for GB4C-128 Packages (Continued)

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO28	UNUSED	I/O	UNUSED	
GPIO29	UNUSED	I/O	UNUSED	



Event



Overt shutdown



Throttle

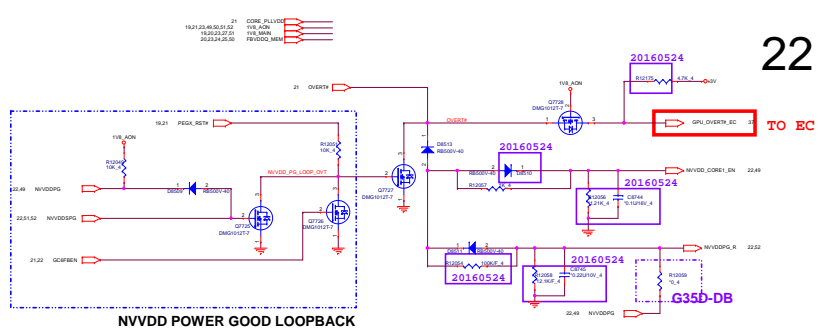
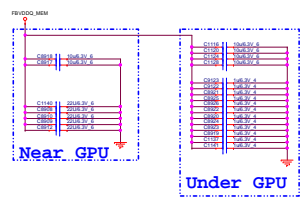
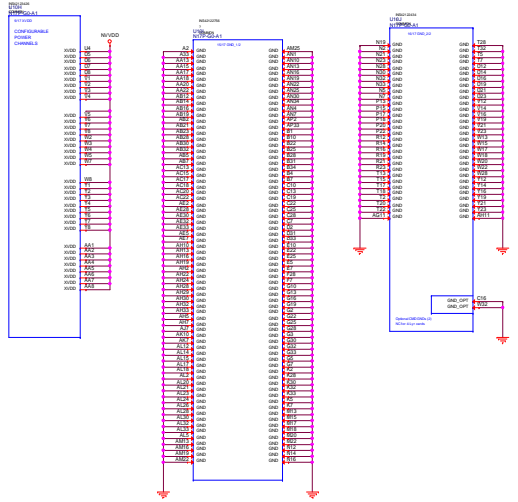


Event



Overt shutdown

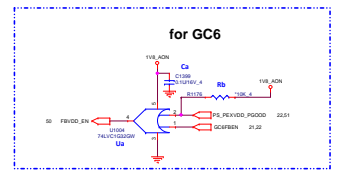




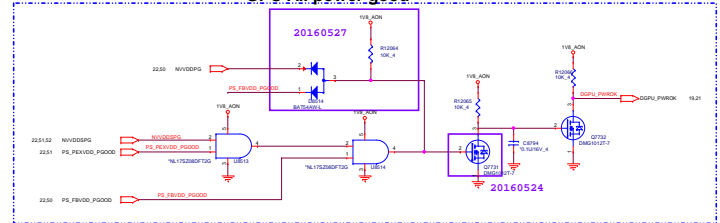
NVVDD POWER GOOD LOOPBACK

GPU All power good

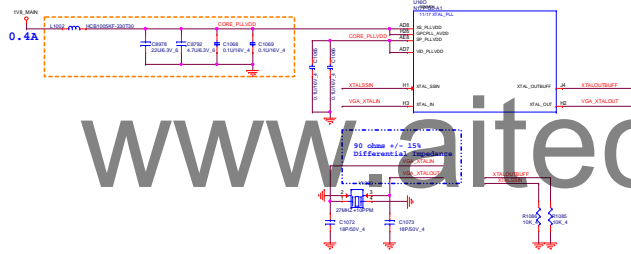
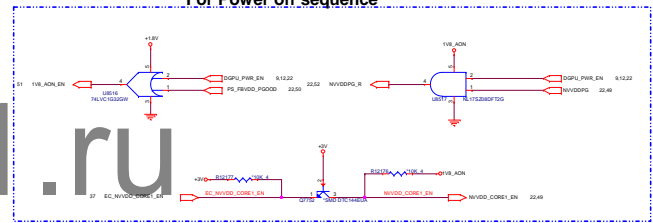
Overt temp ckt for NVVDD and NVVSS



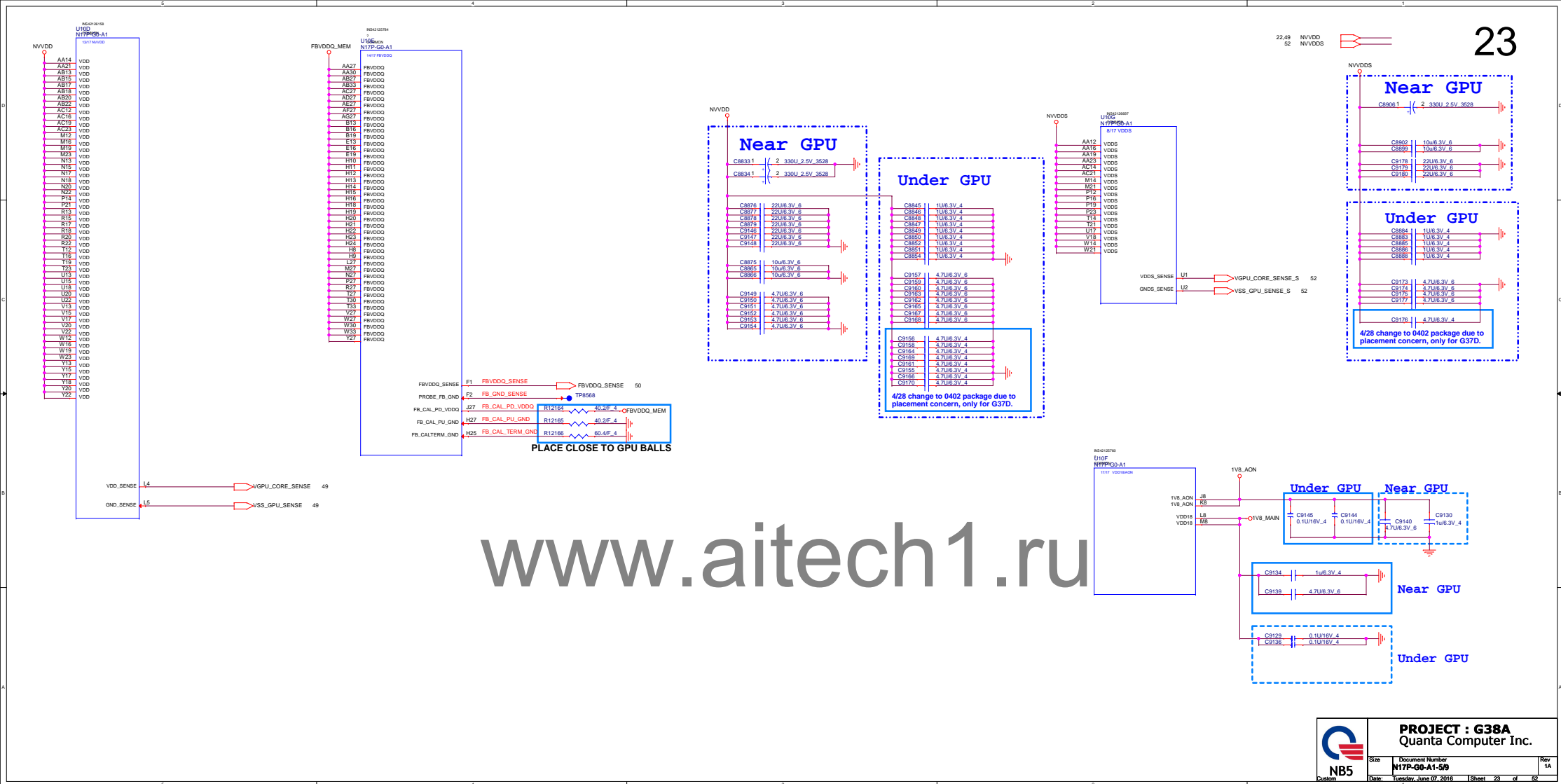
for GC6



For Power off sequence



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Channel 0
<0-31>Channel 1
<32-63>

MF=0 Non-mirrored

MF=1 mirrored

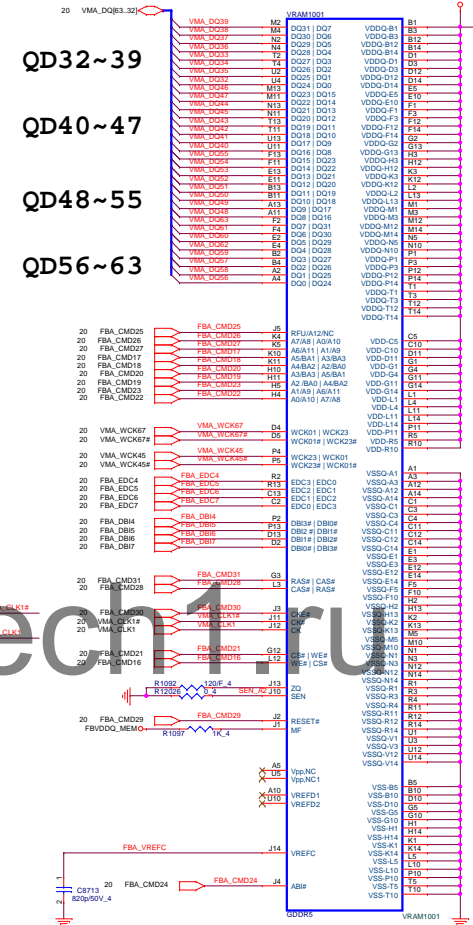
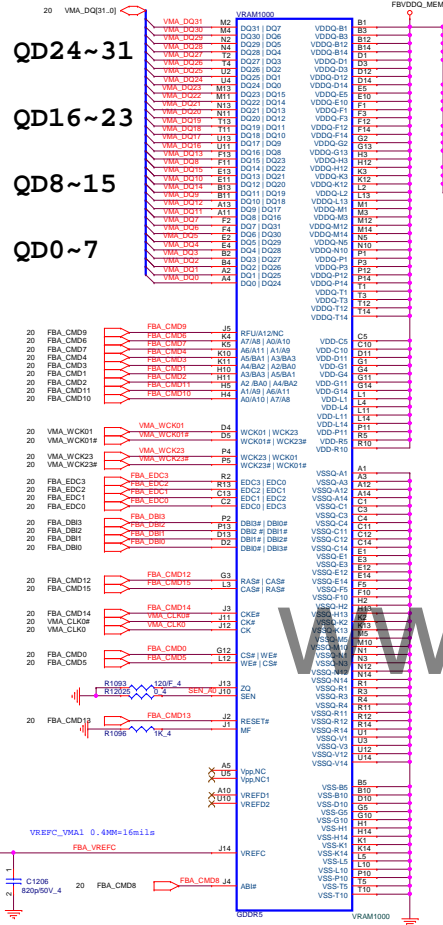


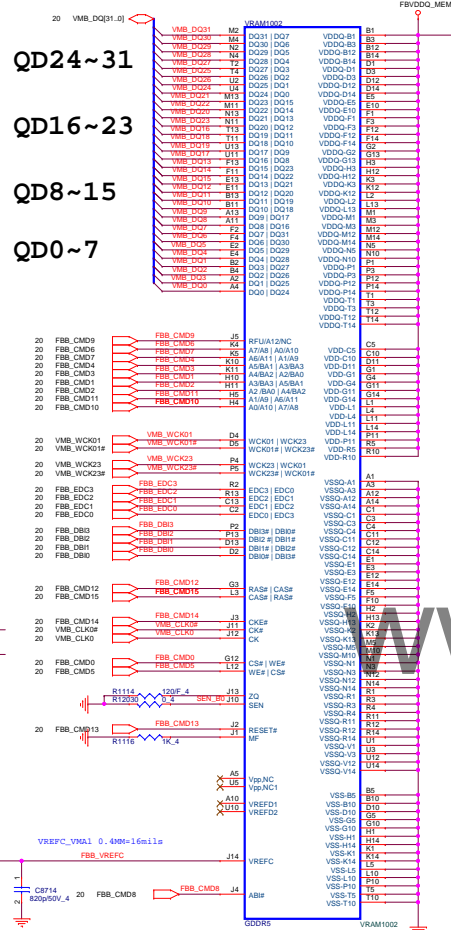
Table 9.4 GDDR5 Command Mapping (GB4C-128 & GB2C-64 packages)

Command Ball on GPU		DRAM Signal Definition	
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]		
FBA_CMD0	FBA_CMD16	CS*	
FBA_CMD1	FBA_CMD17	A3_BA3	
FBA_CMD2	FBA_CMD18	A2_BA0	
FBA_CMD3	FBA_CMD19	A4_BA2	
FBA_CMD4	FBA_CMD20	A5_BA1	
FBA_CMD5	FBA_CMD21	WE*	
FBA_CMD6	FBA_CMD22	A7_A8	
FBA_CMD7	FBA_CMD23	A6_A11	
FBA_CMD8	FBA_CMD24	AB1*	
FBA_CMD9	FBA_CMD25	A12_RFU	
FBA_CMD10	FBA_CMD26	A0_A10	
FBA_CMD11	FBA_CMD27	A1_A9	
FBA_CMD12	FBA_CMD28	RA5*	
FBA_CMD13	FBA_CMD29	RST*	
FBA_CMD14	FBA_CMD30	CKE*	
FBA_CMD15	FBA_CMD31	CAS*	

Table 9.5 GDDR5 DEBUG Command Lines

Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

Channel 0
<0~31>
MF=0 Non-mirrored



Channel 1
<32~63>
MF=1 mirrored

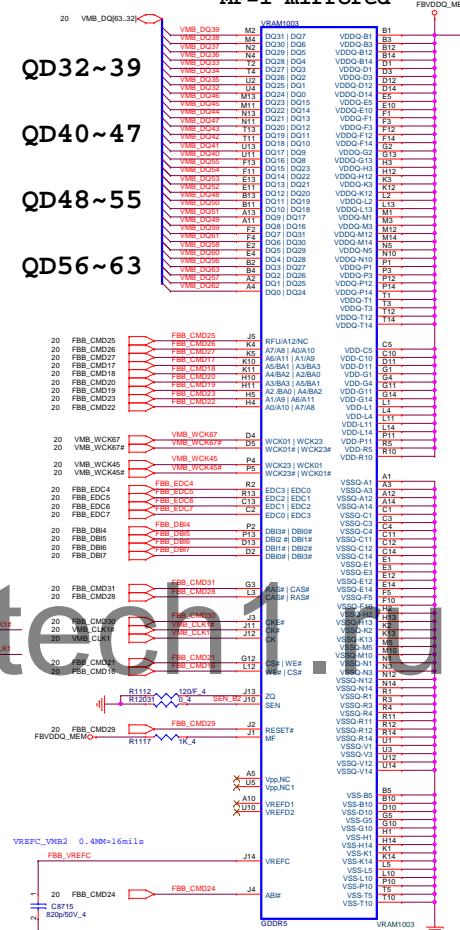


Table 9.4 GDDR5 Command Mapping (GB4C-128 & GB2C-64 packages)

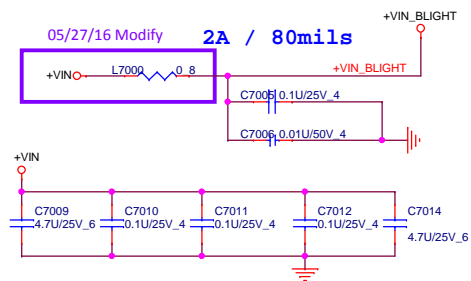
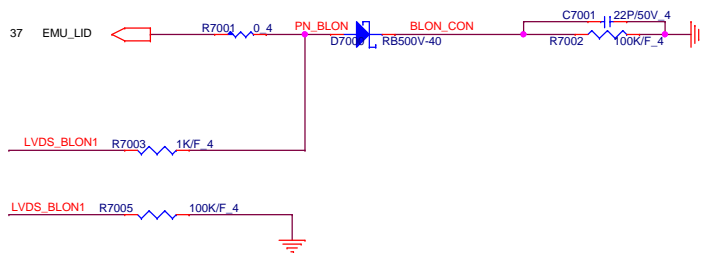
Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	AB1*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

Table 9.5 GDDR5 DEBUG Command Lines

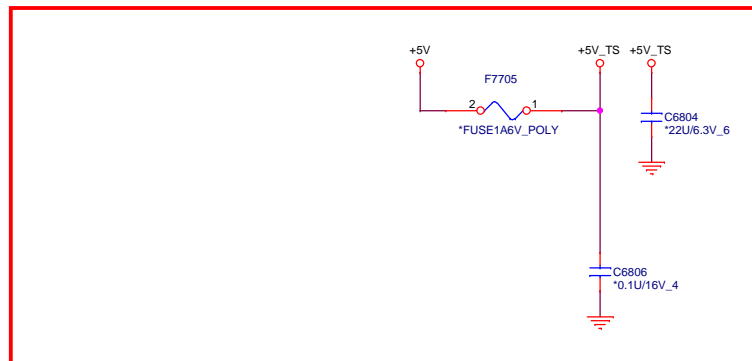
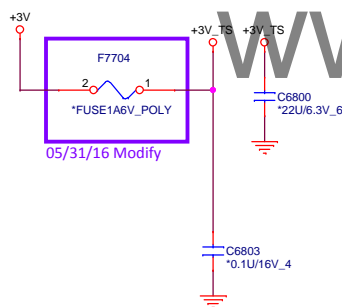
Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

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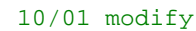
LID Switch



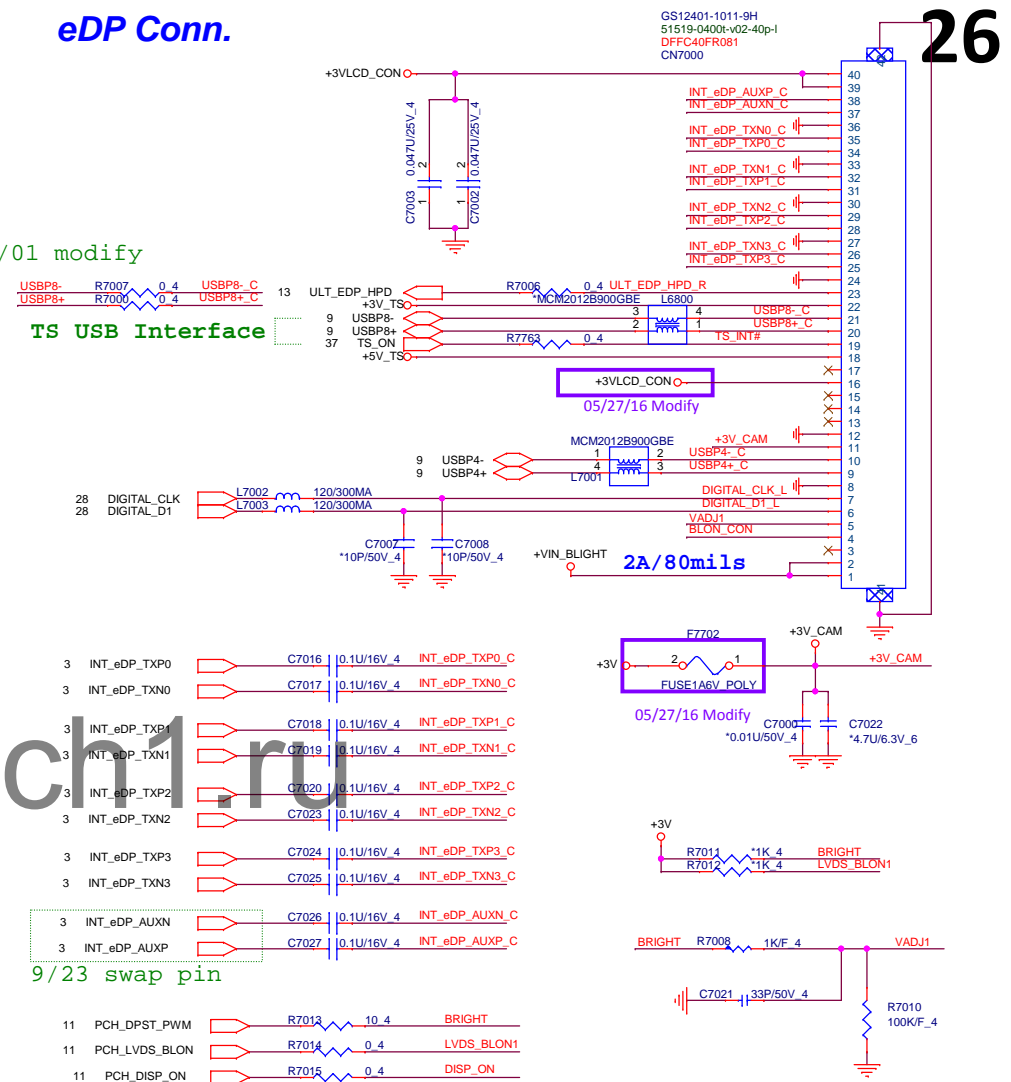
Touch screen



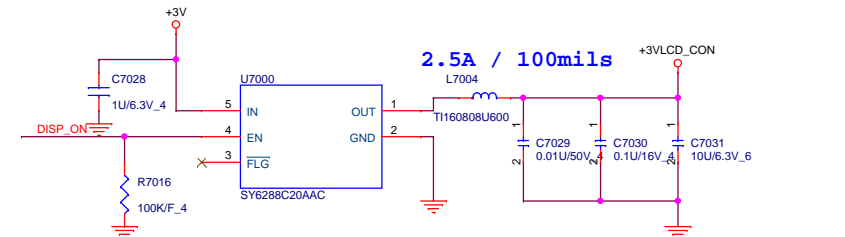
eDP Conn.

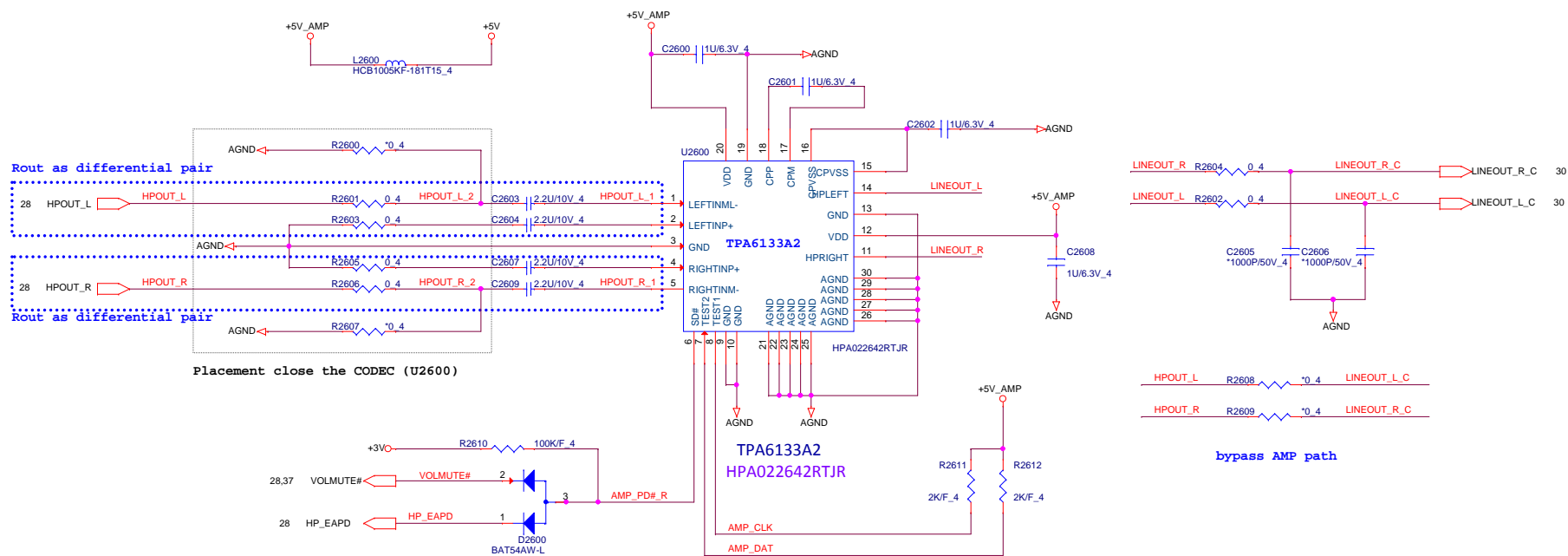


TS USB Interface

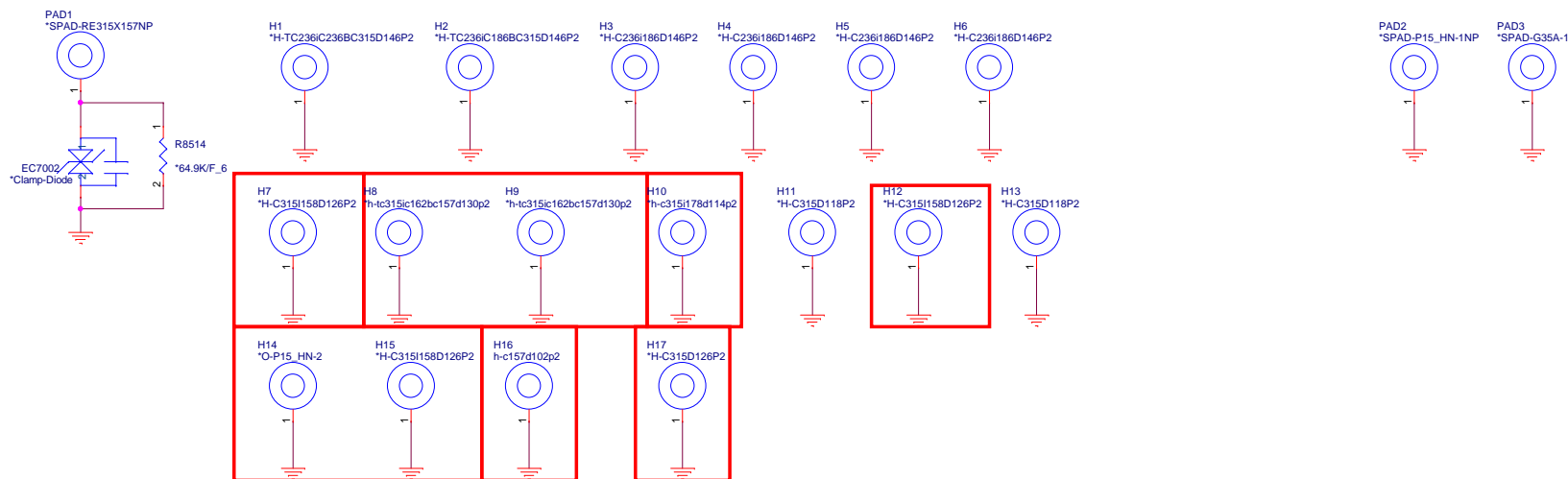


```
9/23 swap pin
```

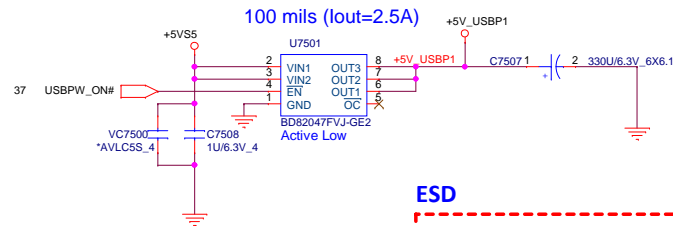




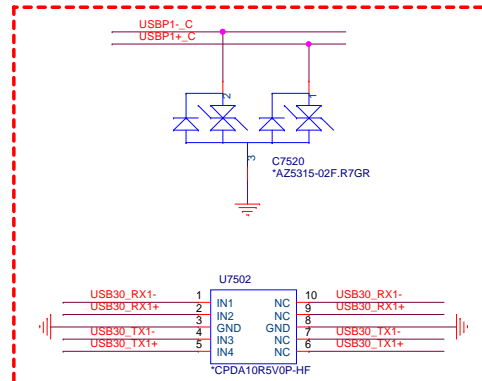
HOLE



USB 2.0/3.0 Combo



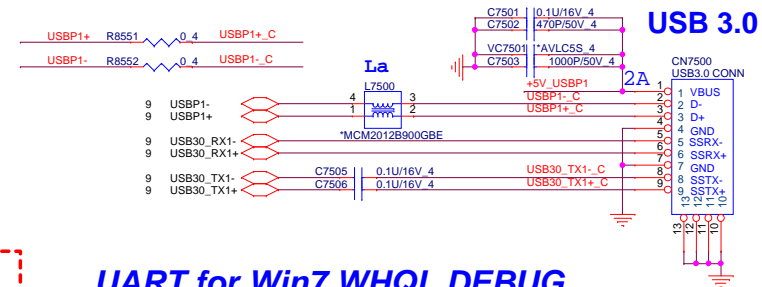
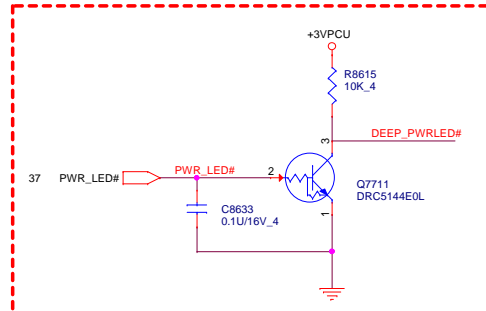
ESD



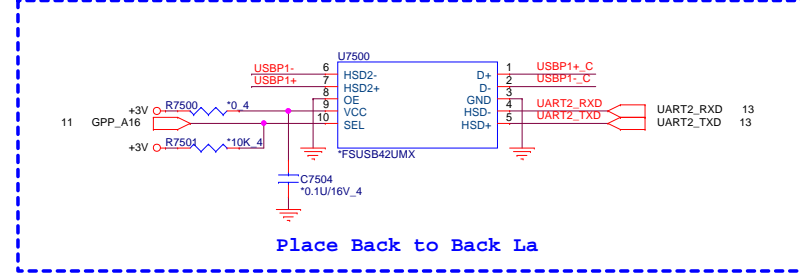
1125 Reserve ESD protection component

Daughter Board

1123 Add PWR LED MOS Circuit

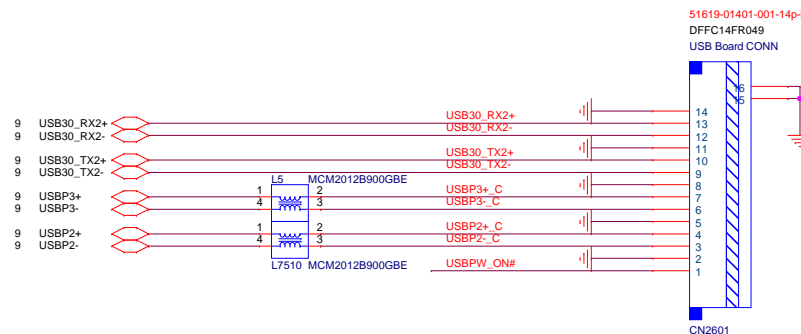
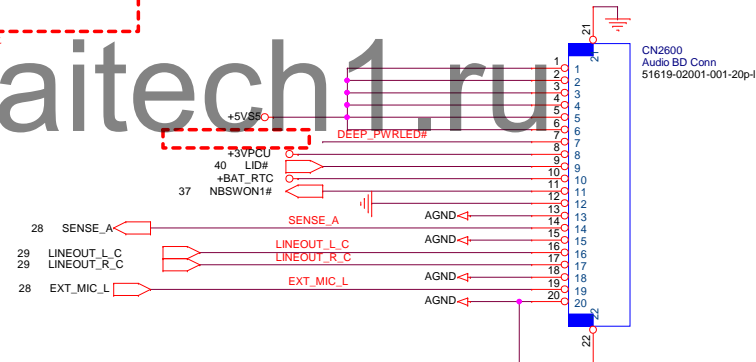


UART for Win7 WHQL DEBUG



Place Back to Back La

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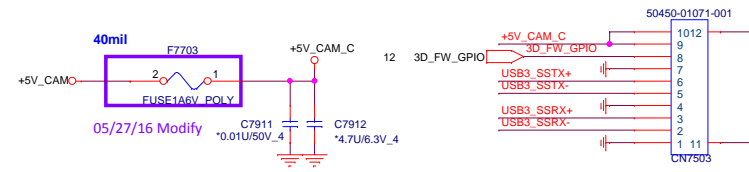


10/08 3D Camera MIC combine in LCD CONN

3D Camera Conn.

USB3.0

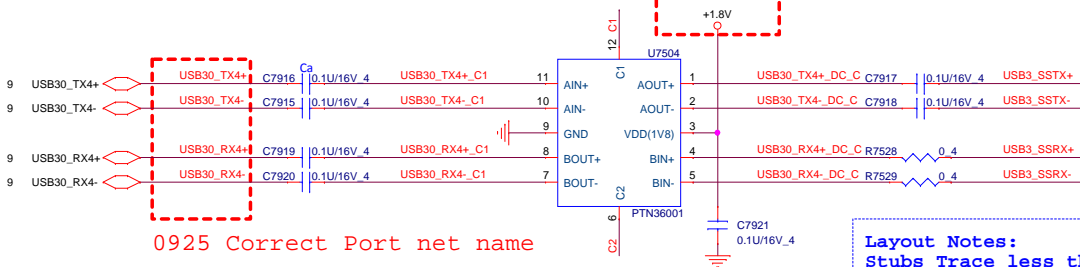
USB3.0 Re-driver IC



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1123 Change UB3 re driver power rail from +1.8V_DEEP_SUS to +1.8V

USB3.0 re-driver IC



Layout Notes:
Stubs Trace less than 150mil

Table 4. C1 pin controls long/medium/short traces

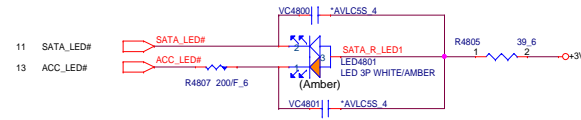
State	Channel type	Pin C1 state	Channel B	Channel A	
			EQ ^[1]	DE ^[2]	OS ^[3]
H	Long	H	9 dB	-5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	-3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

Table 5. C2 pin controls long/medium/short traces

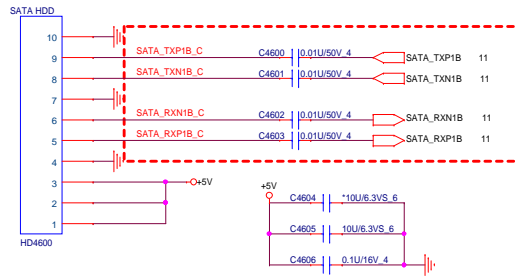
State	Channel type	Pin C2 state	Channel A	Channel B	
			EQ ^[1]	DE ^[2]	OS ^[3]
H	Long	H	9 dB	-5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	-3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

28,40,41,46,51 +5VPCU
5,10,21,30,33,37,38,40,41 +3VPCU
22,28,47,51 +1.8V

SATA LED



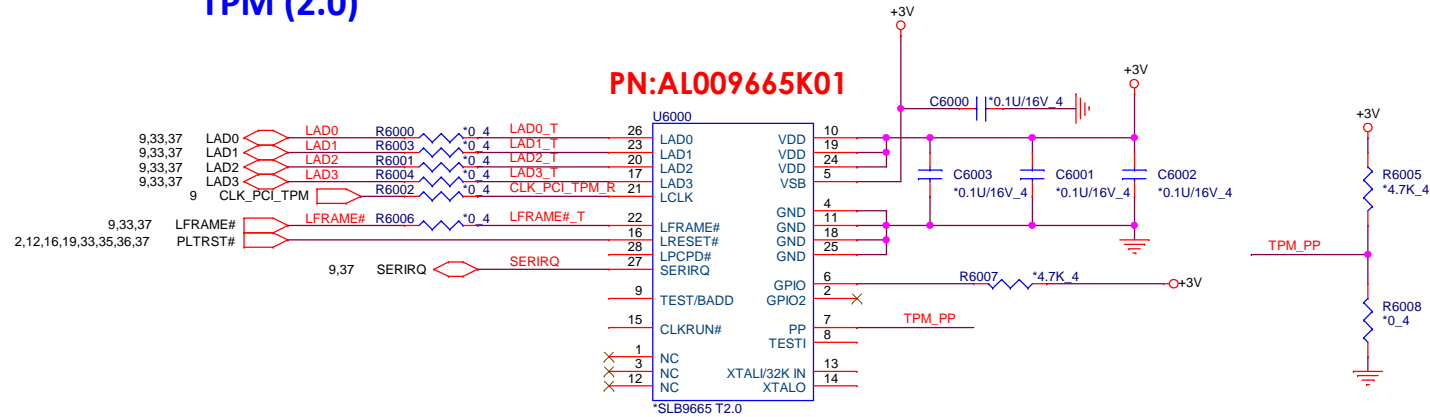
HDD



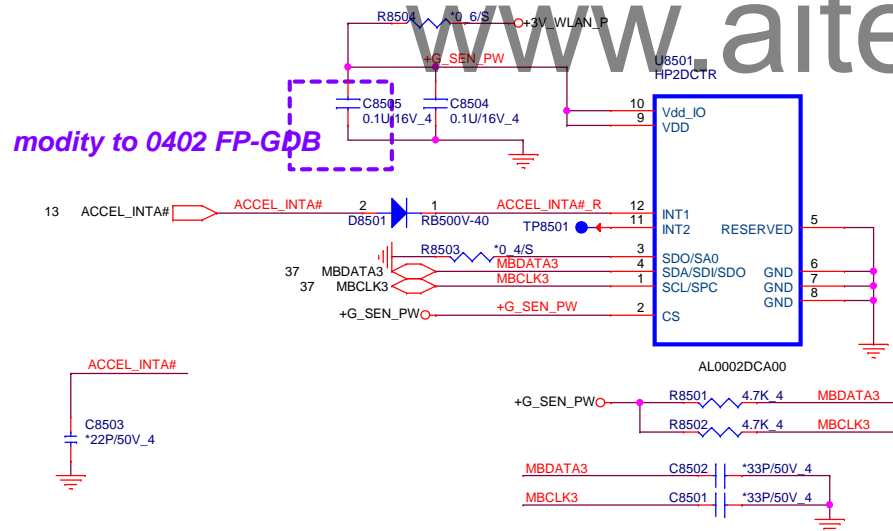
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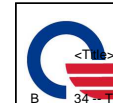
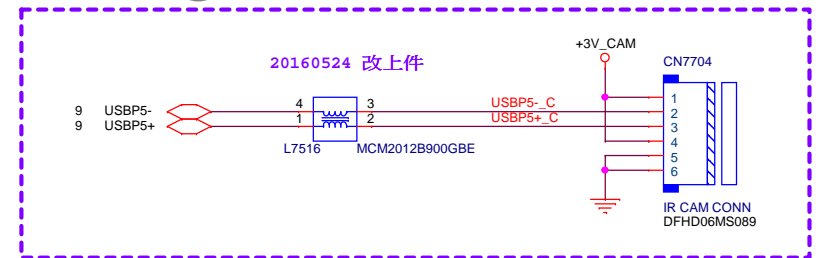
TPM (2.0)



Accelerometer Sensor

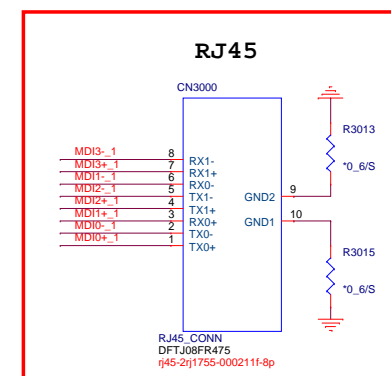
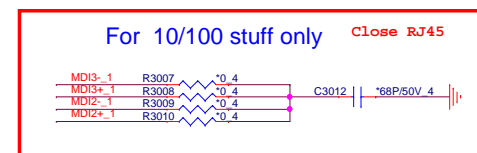
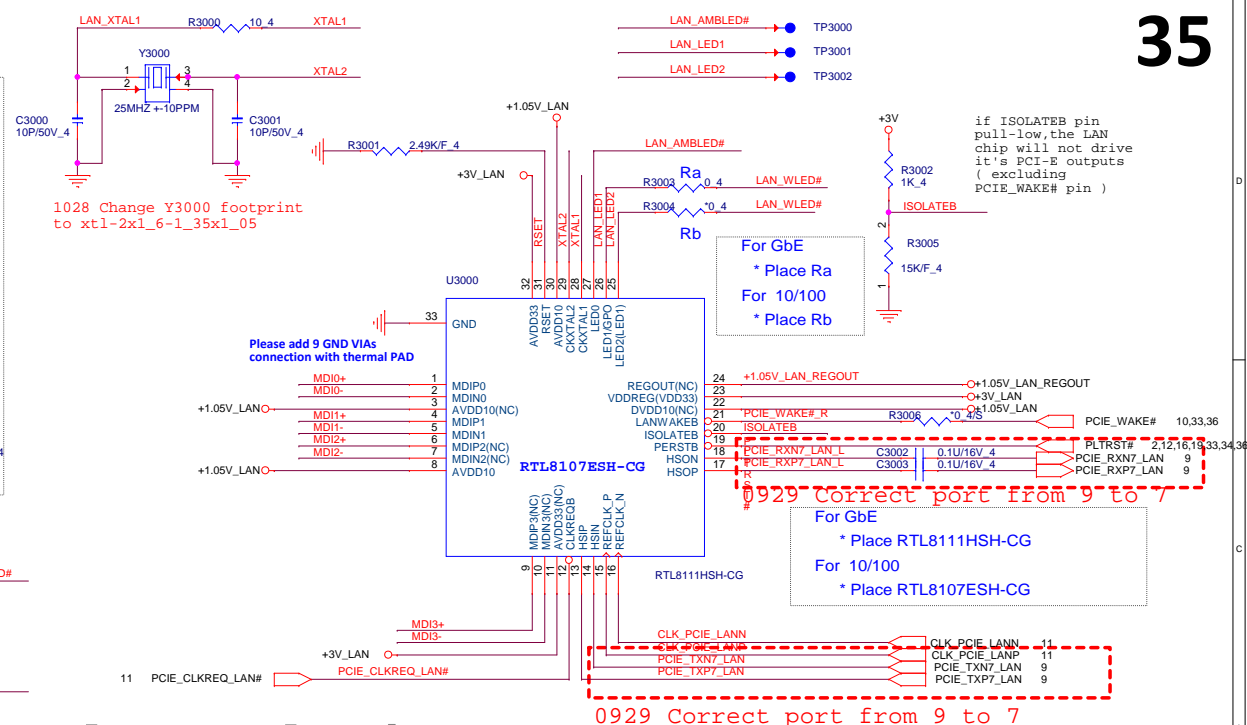
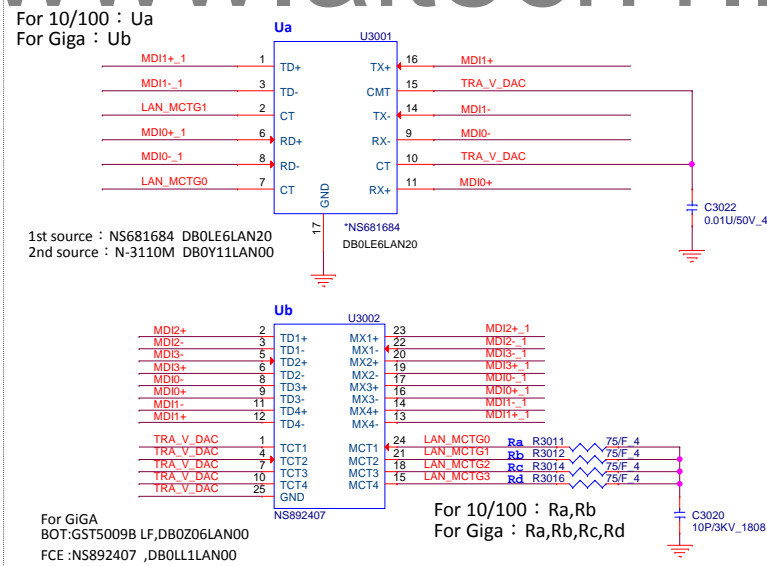
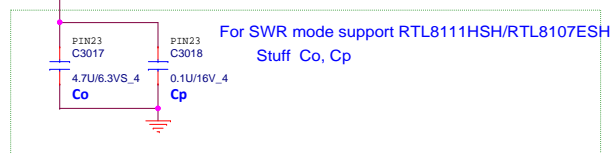
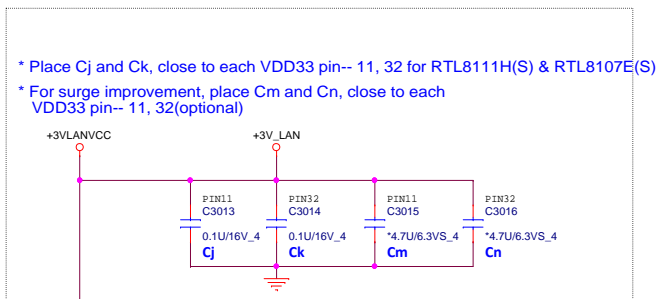
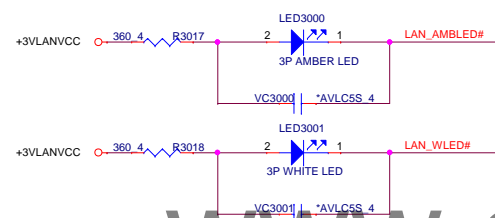
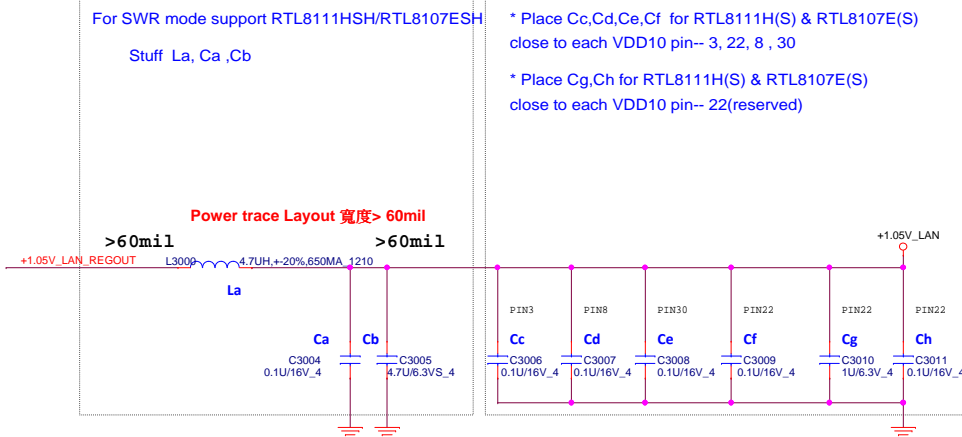


IR CAM



PROJECT : G35
Quanta Computer Inc.

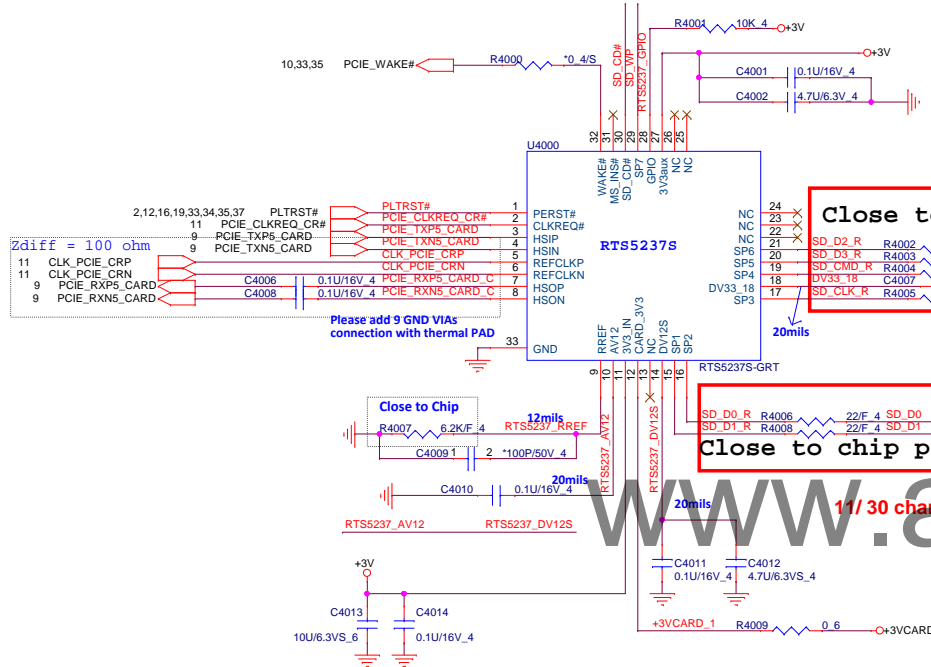
34 - TPM Sensor Document Number 1 Rev
Tuesday, June 07, 2016 34 52
Date: Sheet of



0104 Update footprint

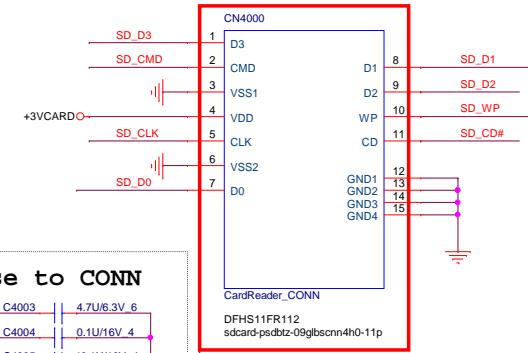
5,9,10,11,12,13,14,16,17,18,22,26,27,28,29,30,32,33,34,35,37,38,43,46,50,51

+3V



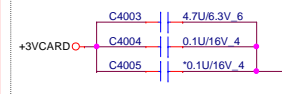
SP1	SD_D1	MS_D1
SP2	SD_D0	MS_D0
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7	SD_WP	MS_DS

Share Pin
SD / MMC



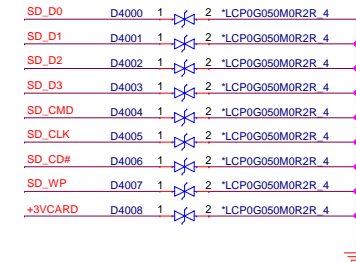
11/ 23 change pin define

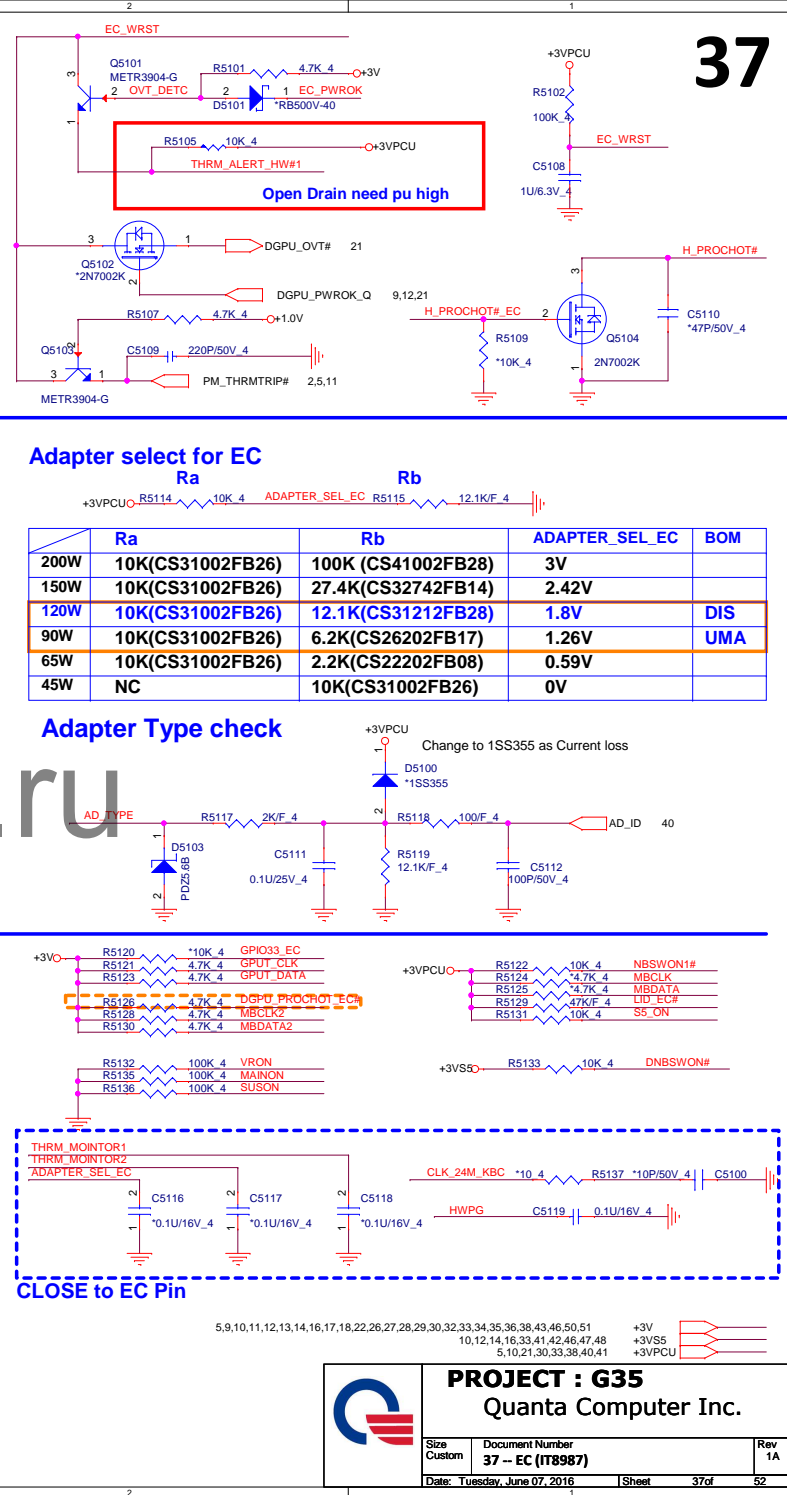
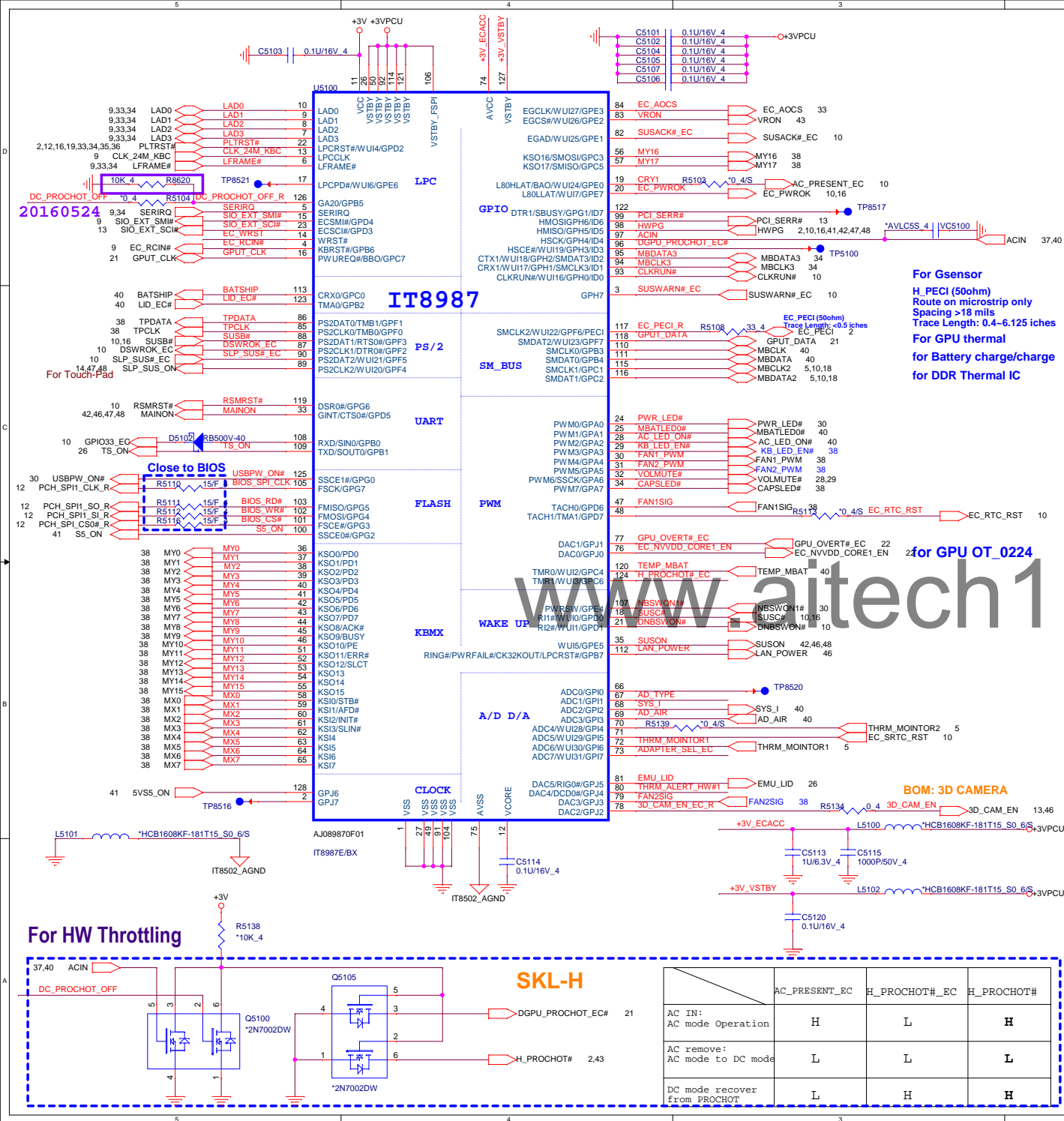
Close to CONN



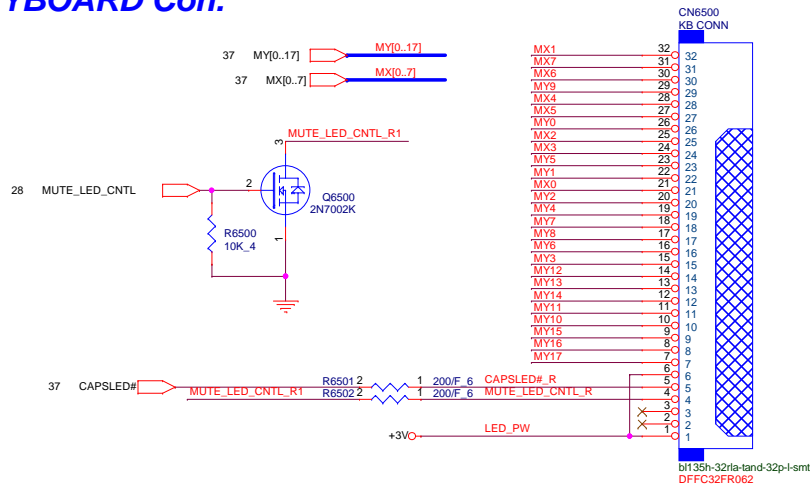
Close to chip

11/ 30 change to 22 ohm & stuff 5.6p for EMI request

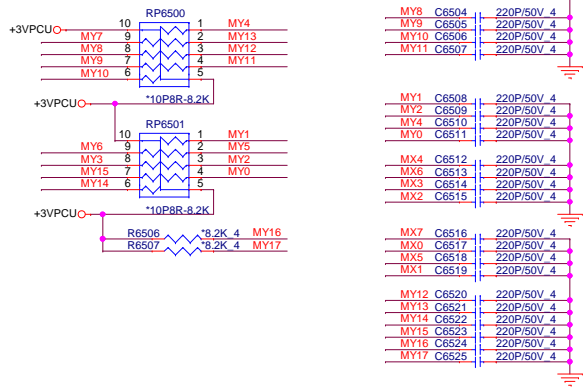




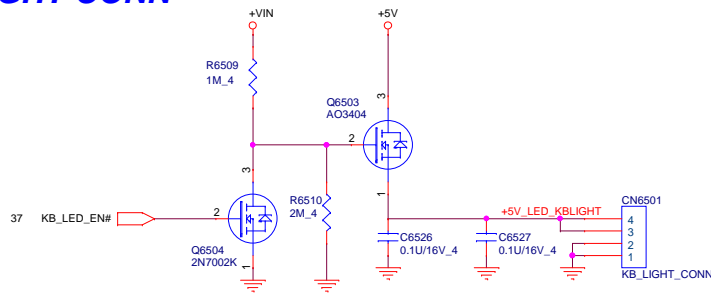
KEYBOARD Con.



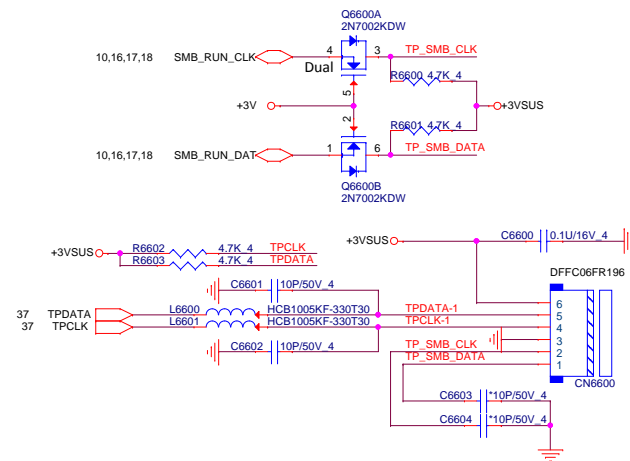
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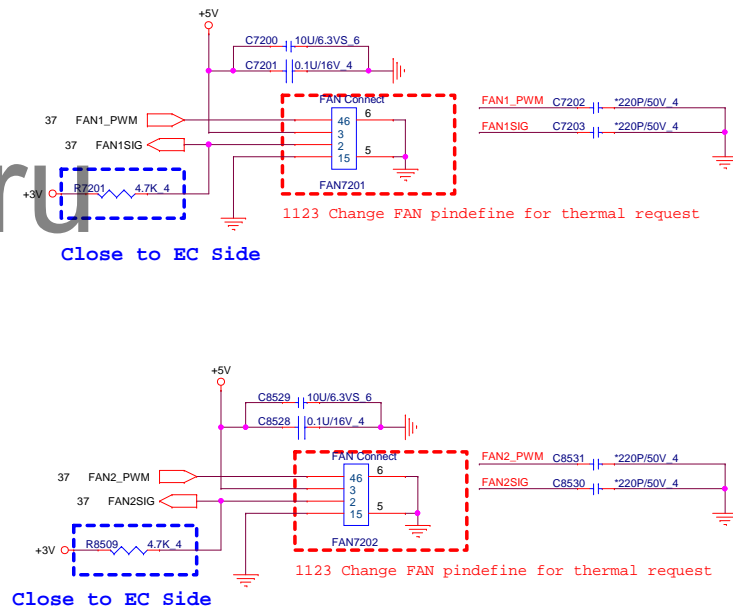
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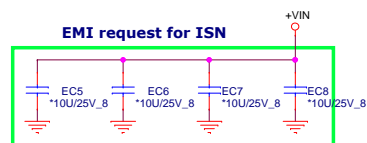
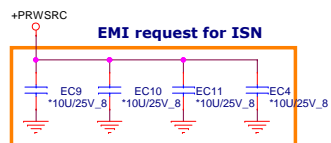


Touch Pad Connector

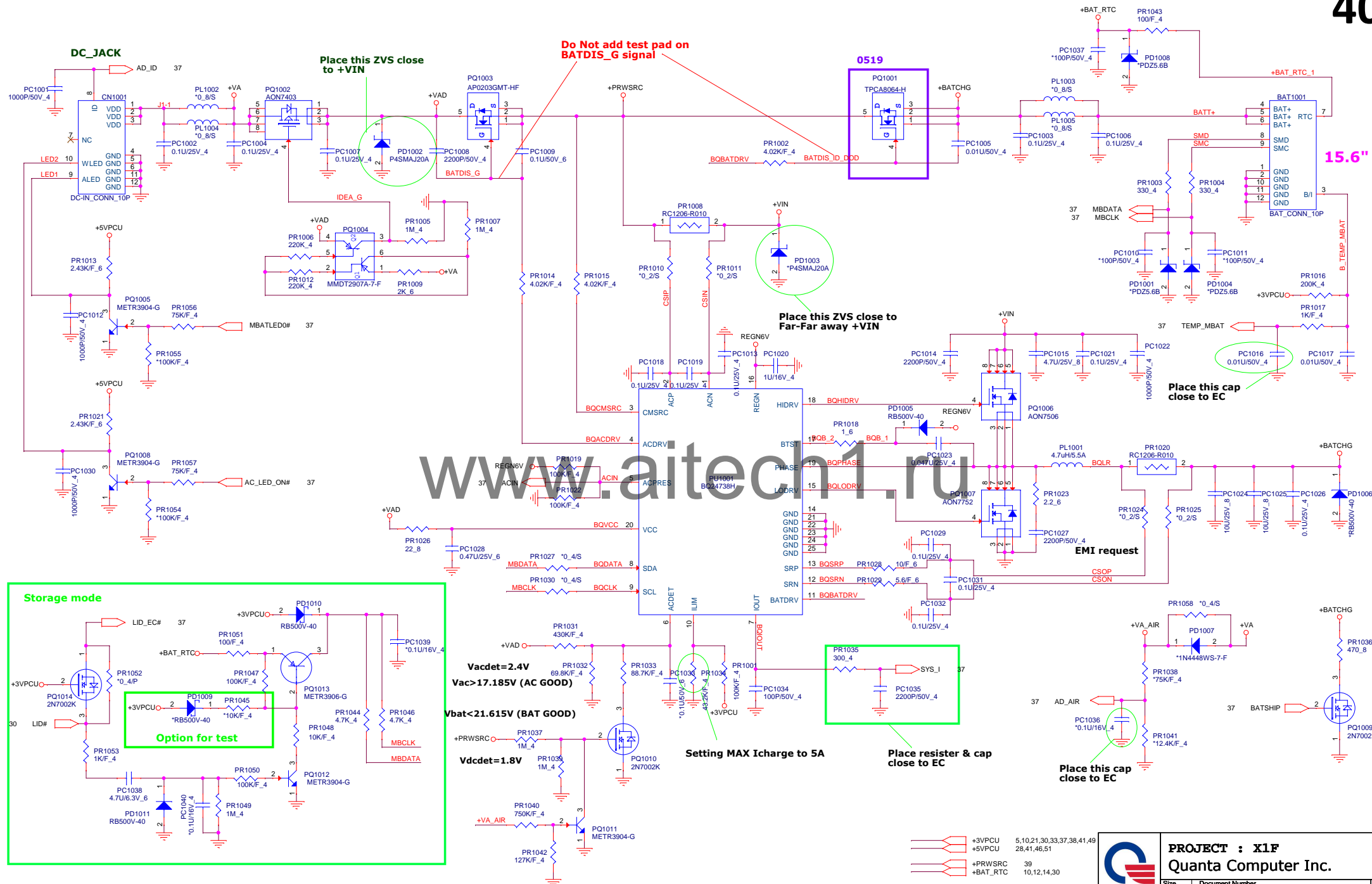


FAN



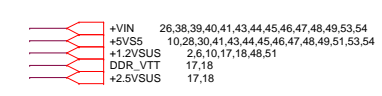


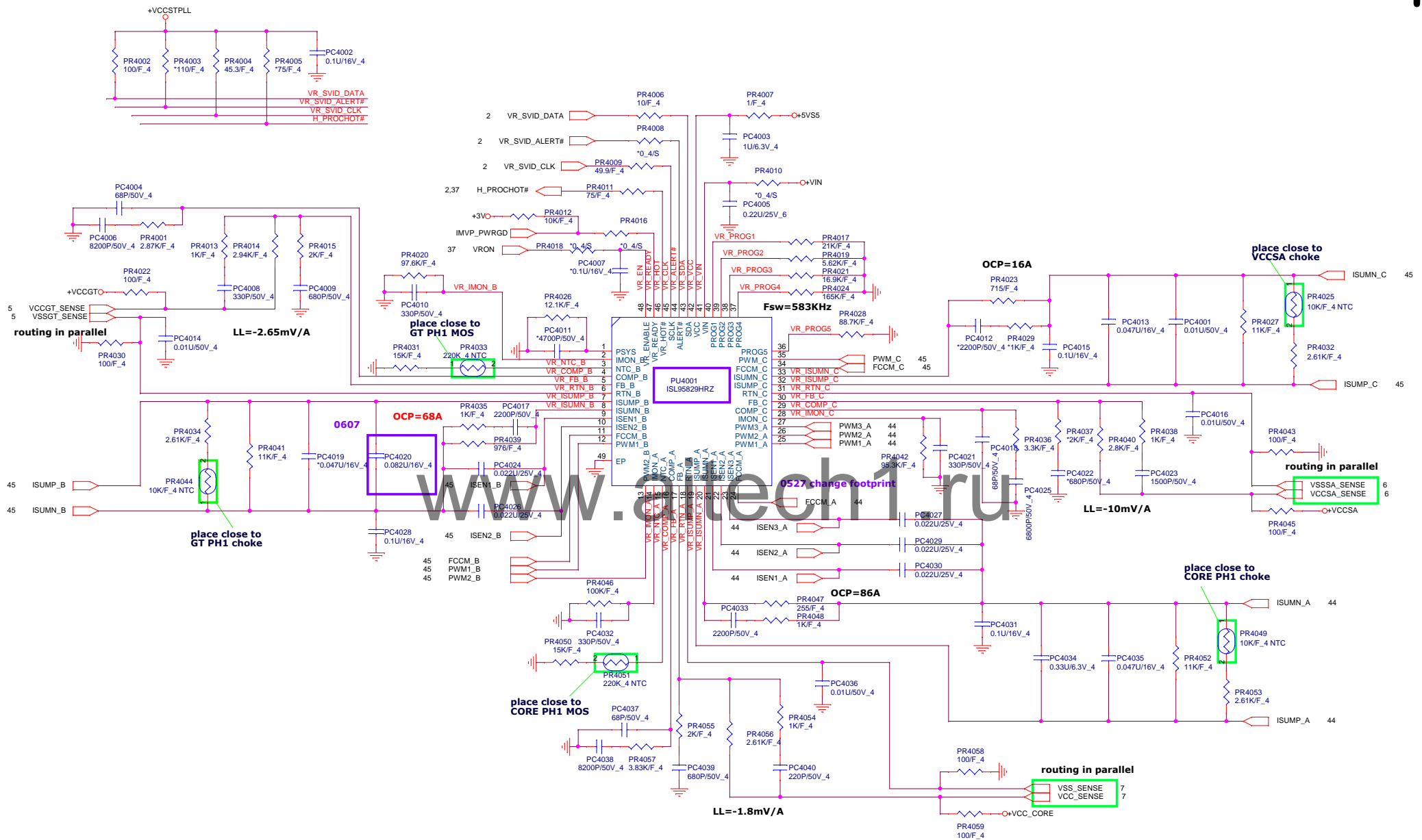
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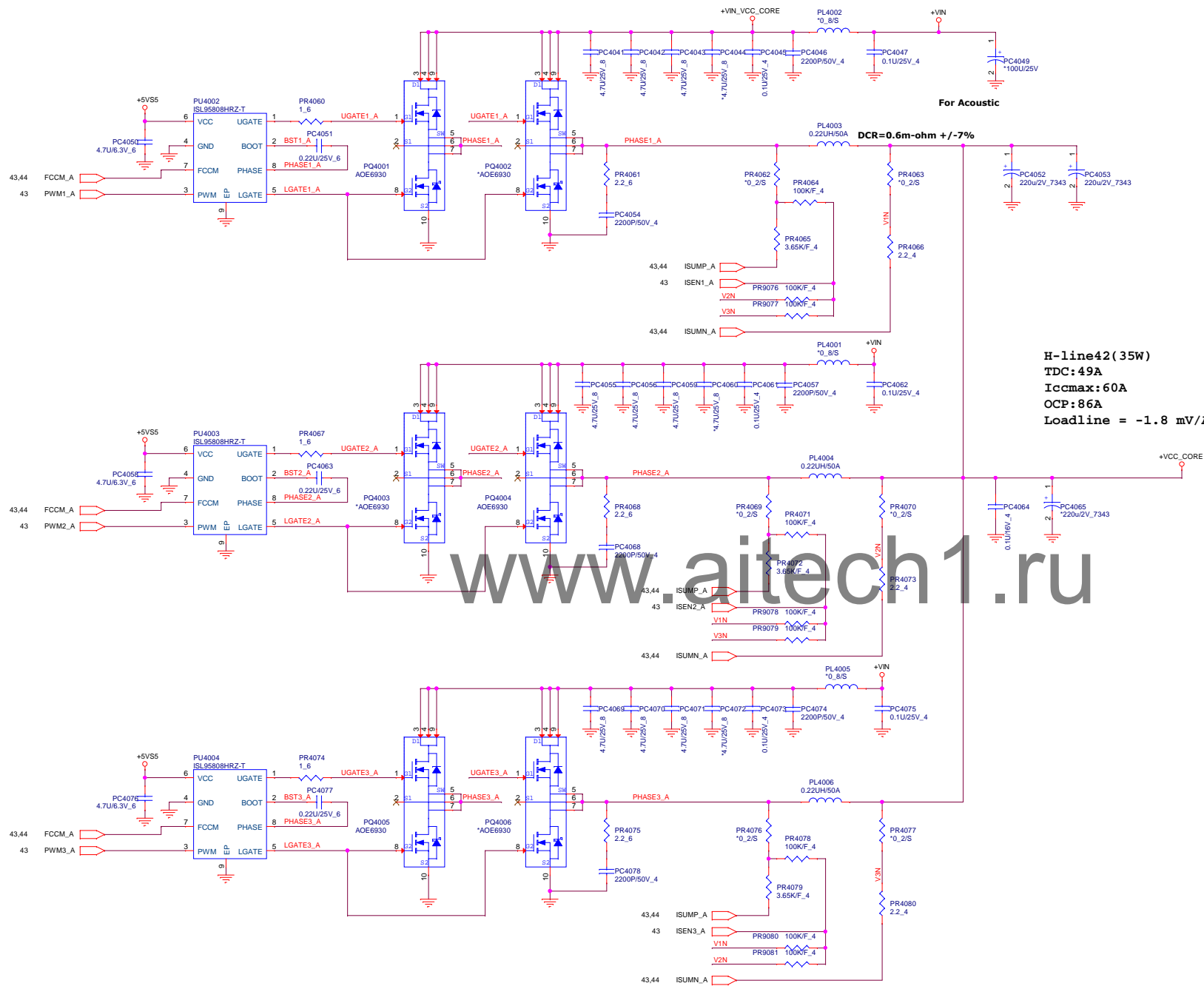


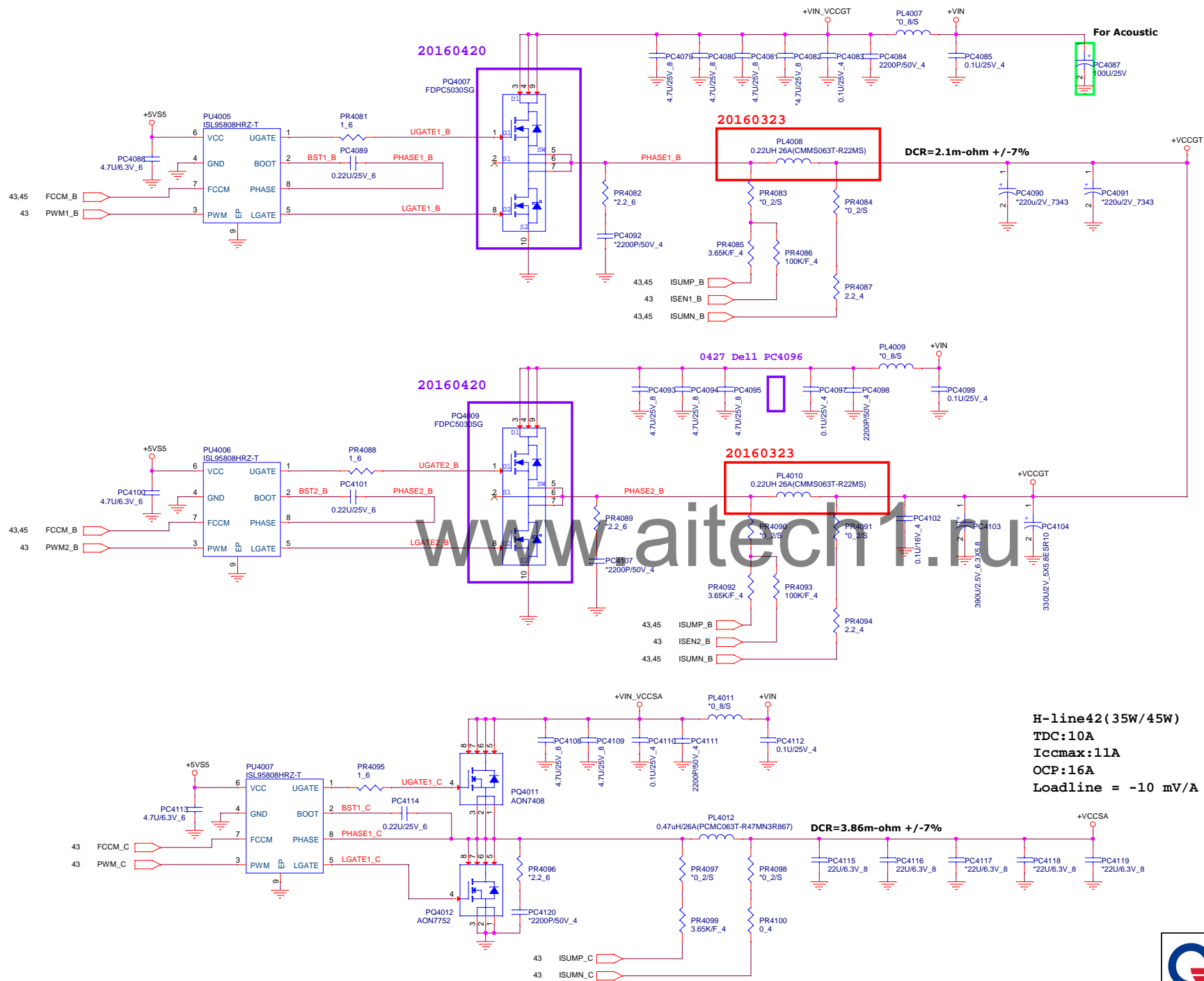


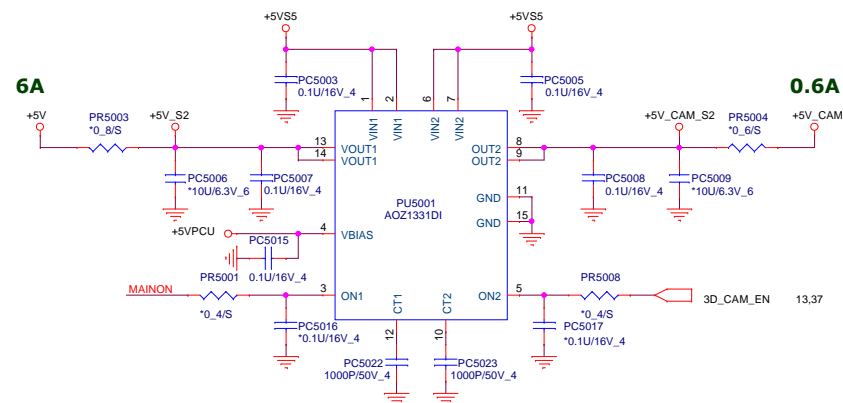
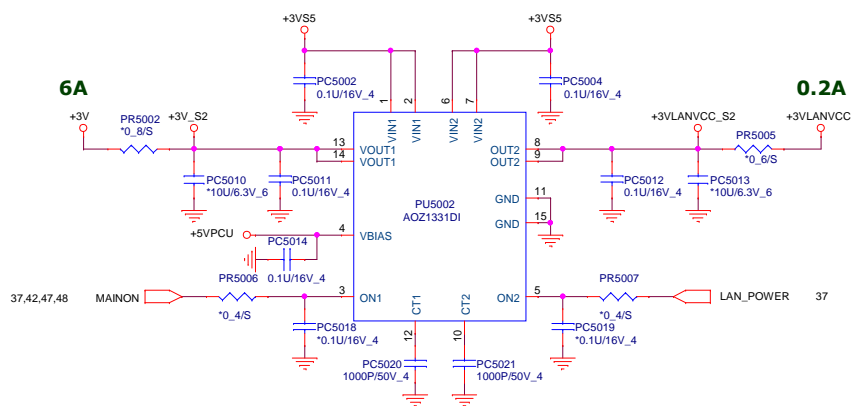
1



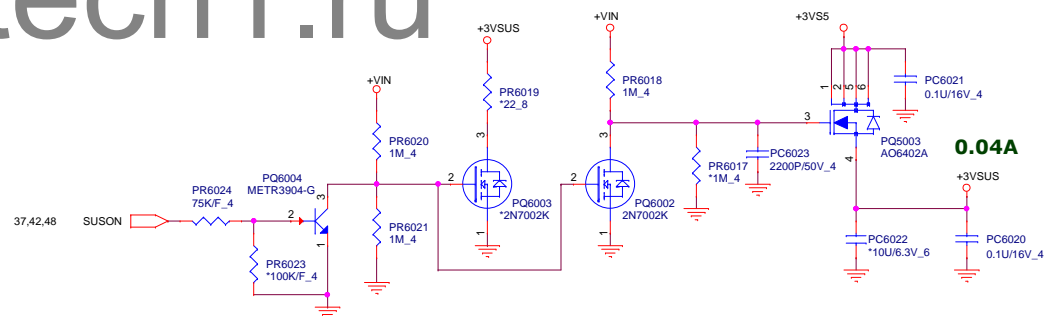







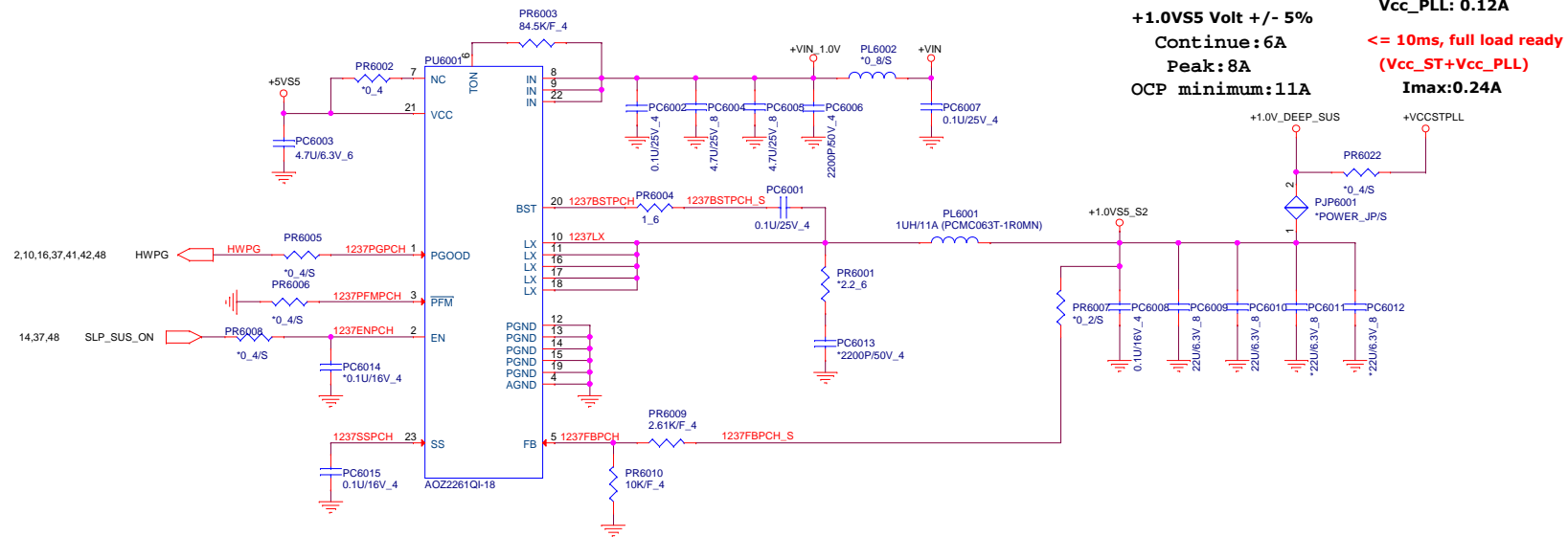


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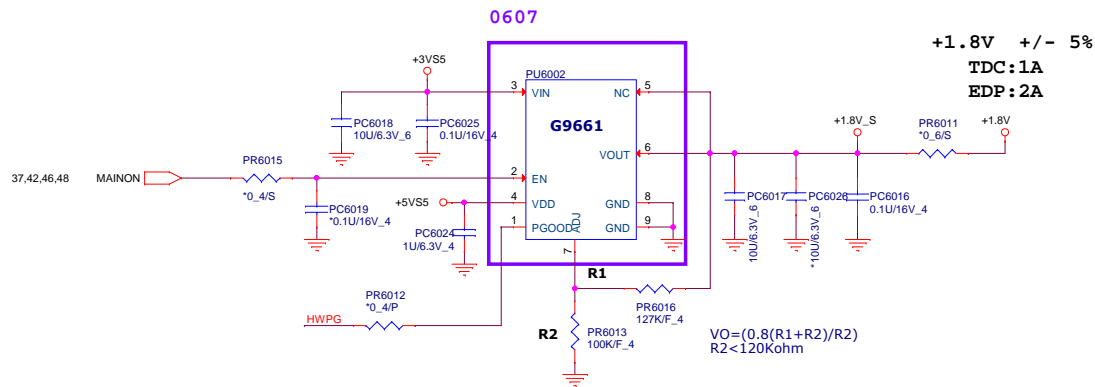


+3V	5,9,10,11,12,13,14,16,17,18,26,27,28,29,30,32,33,34,35,36,37,38,43,54
+5V	26,27,28,29,31,32,38,49
+3VS5	10,12,14,16,33,37,41,42,47,48
+5VS5	10,28,30,41,42,43,44,45,47,48,49,51,53,54
+3VSUS	38
+3VLANVCC	35
+5V_CAM	31
+3V_DEEP_SUS	9,10,12,13,14,16,18


 NB5	PROJECT : X1F		
	Quanta Computer Inc.		
	Size Custom	Document Number	
Load switch IC (AOZ1331D)			Rev 1A
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+VIN	26,38,39,40,41,42,43,44,45,46,48,49,53,54
+3VS5	10,12,14,16,33,37,41,42,46,48
+5VS5	10,28,30,41,42,43,44,45,46,48,49,51,53,54
+1.0V_DEEP_SUS	10,11,14,16,48
+1.8V	22,28,31,51
+VCCSTPLL	2,6,43

 NB5	PROJECT : X1F				
	Quanta Computer Inc.				
	Size Custom	Document Number +1.0_DEEP_SUS			Rev 1A
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Volume Segment

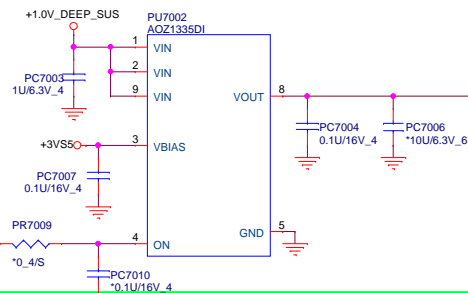
Vcc_STG: 0.04A

Vcc_IO: 5.5A

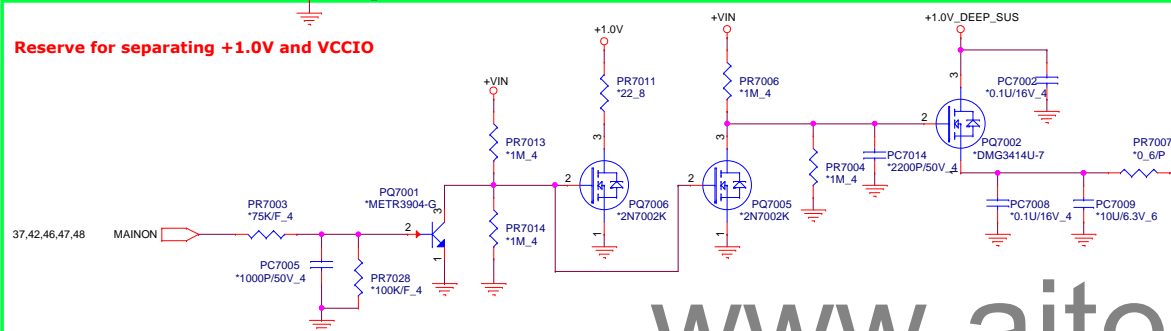
<= 10ms full load ready

Imax:5.5A

Imax:0.04A

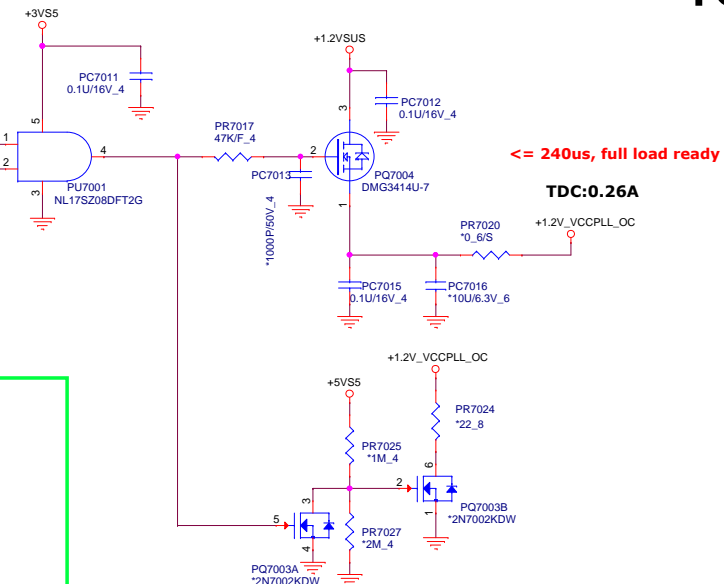
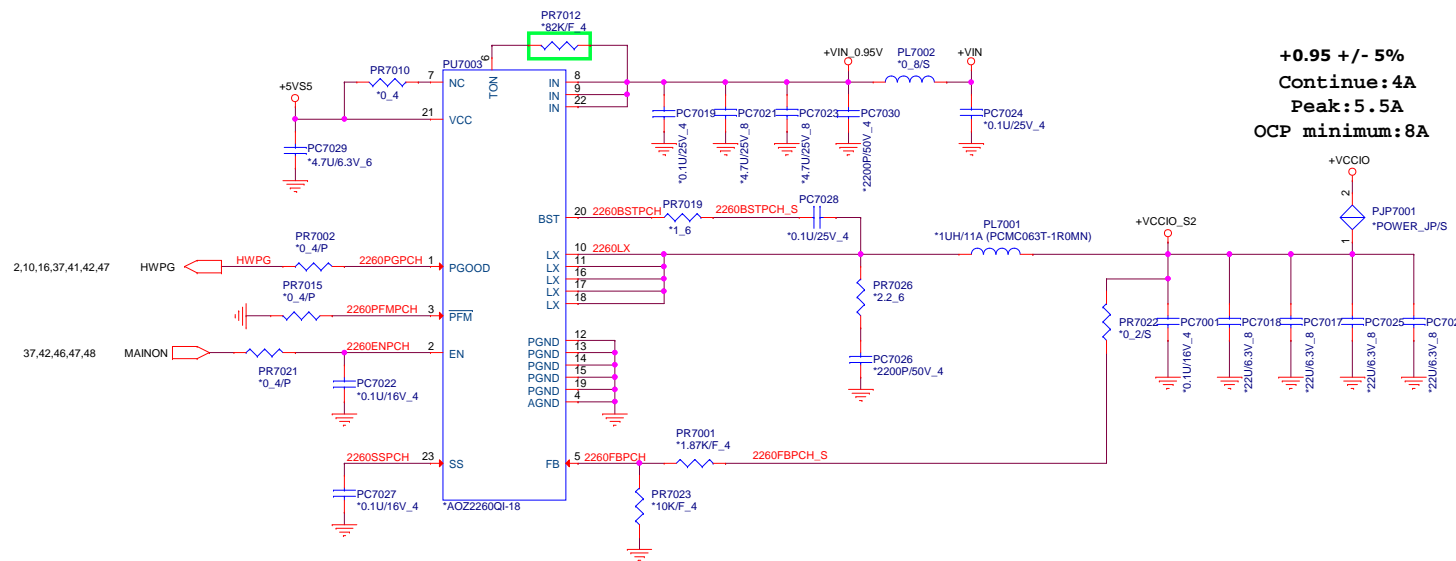


Reserve for separating +1.0V and VCCIO



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+0.95 +/- 5%
Continue:4A
Peak:5.5A
OCP minimum:8A



<= 240us, full load ready

TDC:0.26A

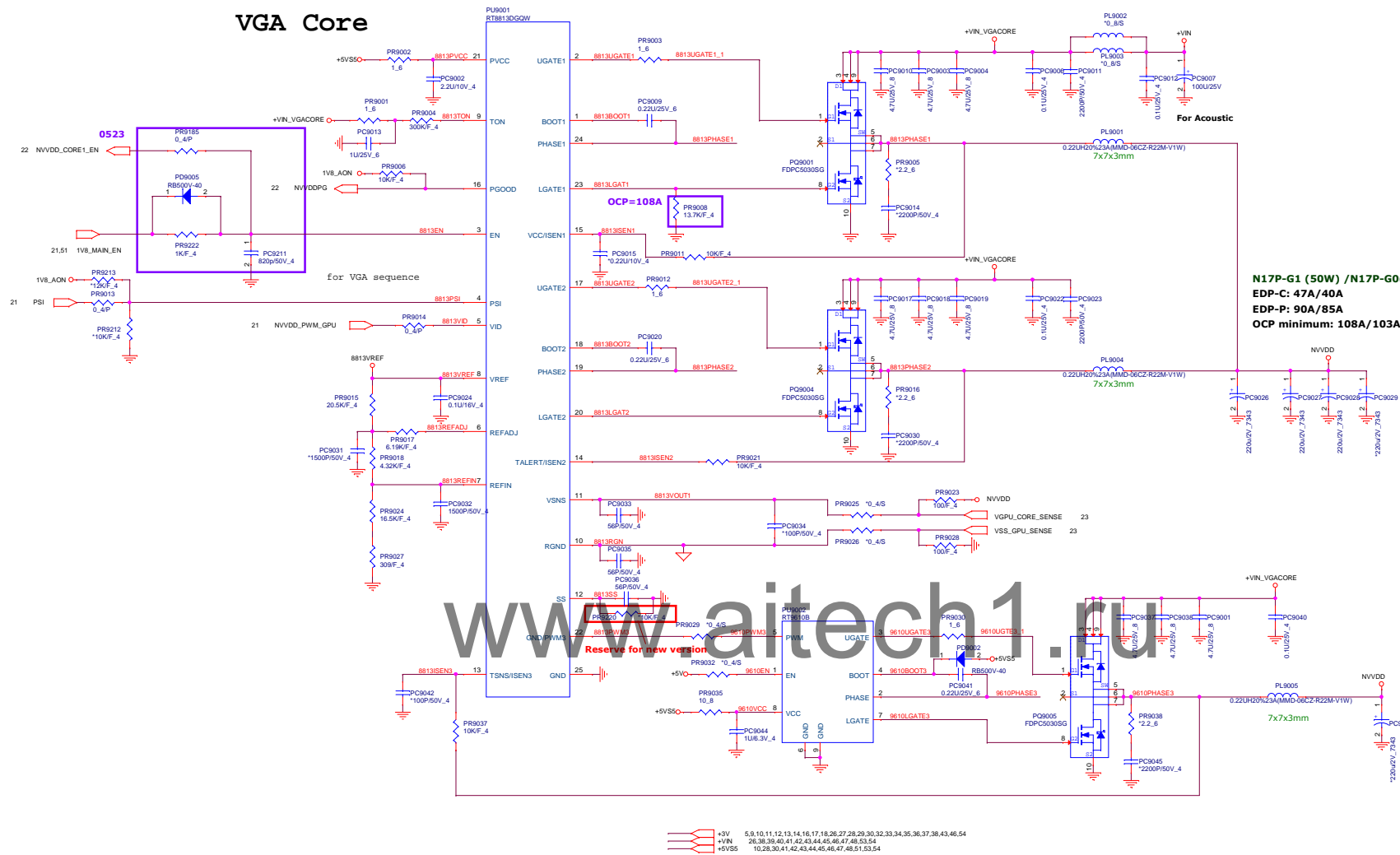
+1.0V	2,5,6,10,16,37
+3VS5	10,12,14,16,33,37,41,42,46,47
+5VS5	10,28,30,41,42,43,44,45,46,47,49,51,53,54
+VCCIO	3,6,16
+1.0V_DEEP_SUS	10,11,14,16,47
+1.2V_VCCPLL_OC	6
+1.2VSUS	2,6,10,17,18,42,51



PROJECT : X1F
Quanta Computer Inc.

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VGA Core



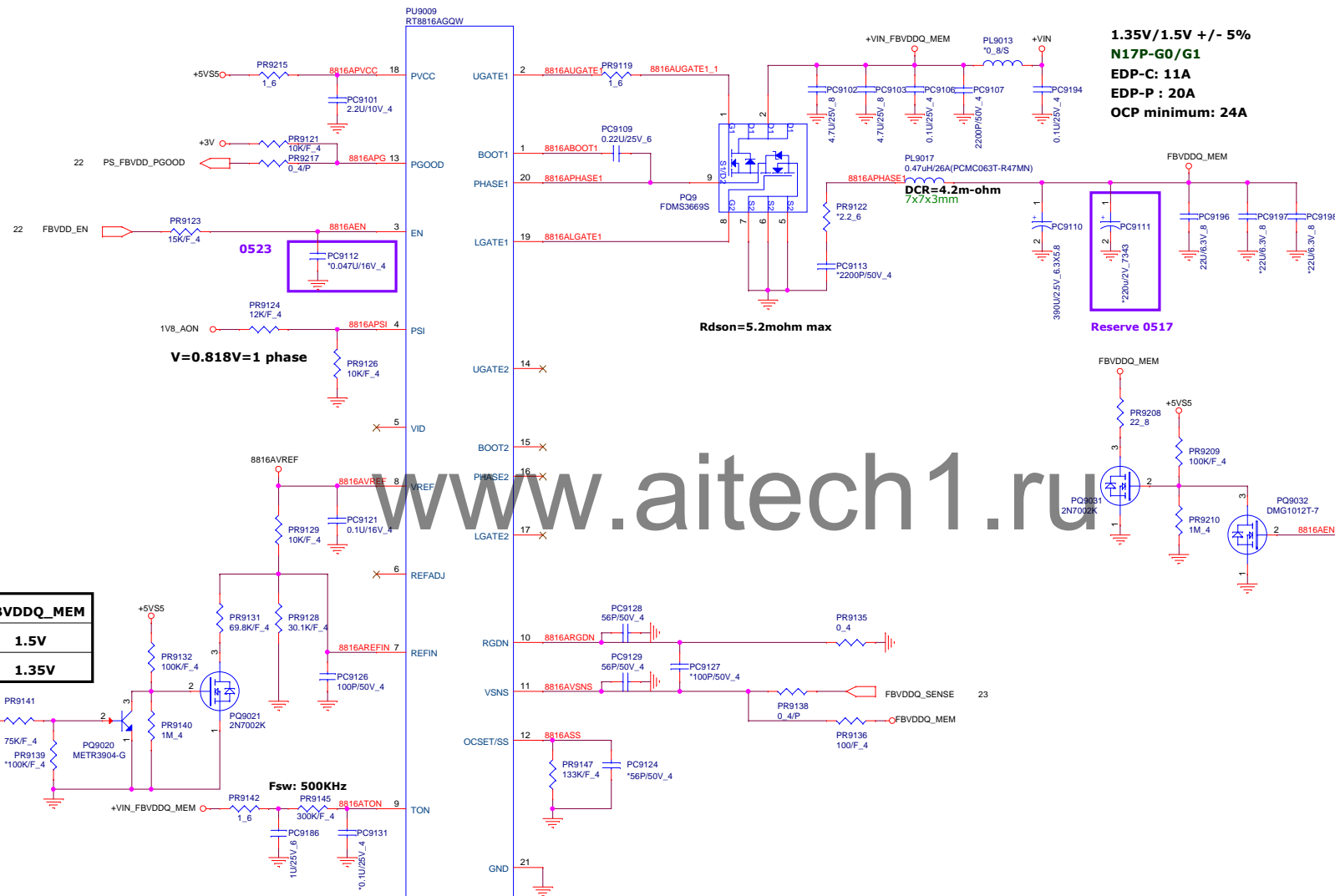
NVDD5

- Ripple Current:**
Irip=7.79A
- Ripple Voltage:**
ESR/1=9mohm
Vrip=70.11mV
- MOSFET Spec:**
L-side MOSFET: FDP5030
Rds(ON)=3mohm (Vgs=4.5 V)
I cont = 25A (T=25 °C)
I pulse=503A
- Frequency:**
F=500KHz (PR9224=300k ohm)
- OCF:**
Set = PR9008 to 13.7K
Vtrip= PR9008*10uA-40mV=97V
Iocp=(Vtrip/Rds(on) + Irip)/2
= 36.23A (1 phase)
Total OCP=36.23*3=108.6A (3 phase)



PROJECT : X1Q
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Size	Document Number	Rev
Custom	+VGACORE (RT8813C)	1A
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FBVDDQ

1. Ripple Current:

Irip=5.34A Vo=1.35V
 Irip=5.88A Vo=1.5V

2. Ripple Voltage:

ESR/1=9mohm
 Vrip=48.06mV Vo=1.35
 Vrip=53mV Vo=1.5

3. MOSFET Spec:

L-side MOSFET: FDM33669S
 Rds(ON)=5.2mohm (Vgs=4.5 V)
 I cont = 18A (T=25 °C)
 I pulse=60A

4. Frequency:

F=500KHz (PR9145=300k ohm)

5. OCP:

Set = PR9147 to 133K Vo=1.35
 Vtrip= PR9147*10uA/12=110.83mV
 I ocp=(Vtrip/Rdson) + I ripple/2 = 24A

+VIN 26,38,39,40,41,42,43,44,45,46,47,48,49,53
 +5VS5 10,28,30,41,42,43,44,45,46,47,48,49,51,53
 FBVDDQ_MEM 20,22,23,24,25



PROJECT : G38A
Quanta Computer Inc.

Size Custom Document Number **+1.35V_GFX (AOZ2263QI-18)** Rev 1A
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